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DESIGN AND ANALYTICAL PERFORMANCE EVALUATION OF A LOW-COST MICROCONTROLLER-BASED DIGITAL OSCILLOSCOPE

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ABSTRACT

Commercial digital storage oscilloscopes remain costly for many teaching laboratories in developing countries. This study presents the design, construction and analytical performance evaluation of a low-cost digital oscilloscope based on the ATmega328P microcontroller, a 128 × 64 graphical liquid crystal display and a switched-mode power supply, built in 2023 at a component cost of ₦51,810 (about US$110). The instrument accepts signals of up to 250 V AC directly through an on-board attenuator, removing the external step-down transformer required by an earlier design. Performance was evaluated from the firmware source code, the design records and recorded functional tests. Although the analogue-to-digital converter is 10-bit in hardware, the firmware reads only its eight most significant bits, giving an effective resolution of 19.53 mV, a quantization uncertainty of ±9.77 mV and a theoretical dynamic range of 49.9 dB. Nine time-base settings from 0.02 to 10 ms/div correspond to nominal sampling rates from 0.8 kS/s up to the converter limit of about 308 kS/s, giving Nyquist limits from 400 Hz to about 154 kHz and a practical display bandwidth of about 30 kHz. In tests with the 220 V, 50 Hz mains supply, the instrument displayed stable sinusoidal traces and reported 50 Hz at the 2, 5 and 10 ms/div settings, consistent with the analysed frequency resolution of 1.25–6.25%. The analysis also shows that reading the full 10-bit result would improve resolution to 4.88 mV and dynamic range to 62 dB without any hardware change.

Keywords: Digital oscilloscope, ATmega328P, Embedded instrumentation, Sampling rate, Quantization error, Low-cost laboratory equipment.

1 INTRODUCTION

Digital oscilloscopes have become indispensable instruments for observing, measuring, and analysing electrical signals across virtually every field of electrical and electronic engineering. Their applications extend from analogue circuit analysis and embedded systems development to telecommunications, biomedical instrumentation, industrial automation, power electronics, and modern Internet of Things (IoT) technologies. By converting analogue signals into digital representations, modern oscilloscopes provide accurate waveform visualization, automated parameter measurements, signal storage, and advanced analytical capabilities that greatly enhance engineering diagnostics and system development [1, 2].

Unlike conventional analogue oscilloscopes, digital oscilloscopes employ analogue-to-digital converters (ADCs) to sample continuous electrical signals at discrete time intervals before reconstructing them for digital display. Consequently, the performance of a digital oscilloscope is fundamentally determined by several critical parameters, including sampling frequency, ADC resolution, analogue front-end design, memory architecture, triggering mechanisms, and display resolution. Among these parameters, sampling frequency and ADC resolution exert the greatest influence on measurement accuracy, waveform fidelity, bandwidth, and overall instrument performance [3, 4].

The theoretical basis for digital signal acquisition is established by the Nyquist–Shannon sampling theorem, which states that a continuous signal can be reconstructed accurately only when sampled at a frequency at least twice its highest frequency component. Sampling below this limit introduces aliasing, causing higher-frequency components to appear as lower-frequency signals and thereby producing misleading waveform representations. Consequently, careful consideration of sampling frequency is essential during oscilloscope design to ensure accurate measurement and signal reconstruction [5, 6, 7].

ADC resolution also plays a critical role in determining oscilloscope performance. The number of quantization levels available within an ADC defines the minimum detectable voltage increment and directly affects measurement precision, quantization noise, and dynamic range. Higher-resolution converters provide improved voltage discrimination but generally require increased hardware complexity, processing capability, and financial investment. Therefore, selecting an appropriate ADC architecture involves balancing measurement accuracy with system cost and implementation complexity [1, 8].

Although commercial digital storage oscilloscopes provide high sampling rates, extensive memory depth, sophisticated triggering systems, protocol decoding, digital signal processing capabilities, and wide bandwidths, their acquisition costs remain prohibitive for many educational institutions, research laboratories, and hobbyist developers, particularly within developing economies. In Nigeria, for example, a 50 kHz oscilloscope cost more than ₦100,000 in 2023 [9]. The financial burden associated with purchasing and maintaining commercial instruments has motivated growing interest in the development of affordable embedded measurement systems capable of satisfying fundamental laboratory requirements [4, 10].

Recent advances in embedded systems have significantly expanded the capabilities of low-cost microcontrollers. Devices such as the ATmega328P integrate multi-channel 10-bit ADCs, programmable timers, interrupt systems, serial communication interfaces, and sufficient processing resources to implement compact data acquisition and measurement systems using minimal external hardware. These features have encouraged numerous researchers to investigate microcontroller-based oscilloscopes for educational applications and low-frequency signal analysis [11, 12].

Previous investigations have demonstrated the feasibility of constructing inexpensive digital oscilloscopes using various embedded platforms [13, 14]. An earlier ATmega328P-based oscilloscope developed in the same department required an external step-down transformer before high voltages could be measured [15]. However, many reported implementations primarily emphasize hardware realization while providing limited quantitative analysis of measurement performance. In particular, evaluations that connect the firmware implementation to the resulting resolution, sampling limits, dynamic range, and measurement uncertainty remain relatively scarce. Consequently, a need exists for studies that combine practical embedded hardware implementation with quantitative performance assessment.

The present study addresses this gap by presenting the design, construction and analytical performance evaluation of a low-cost digital oscilloscope based on the ATmega328P microcontroller. The prototype was designed and built in 2023 as an undergraduate final-year project in the Department of Electronics and Computer Engineering, Nnamdi Azikiwe University [9, 16]. It measures signals of up to 250 V AC directly, without an external transformer. This paper evaluates the instrument from its firmware source code, design records and recorded test results, and quantifies the parameters that govern its measurement capability.

Specifically, this study develops analytical models for: sampling frequency and Nyquist bandwidth at each time-base setting; effective ADC resolution and voltage sensitivity; quantization uncertainty; dynamic range; frequency measurement range and resolution; and waveform scaling on the display.

The analysis shows that, although the ATmega328P ADC is 10-bit in hardware, the firmware stores only the eight most significant bits, which sets the effective resolution at 19.53 mV and the dynamic range at 49.9 dB. The nine time-base settings correspond to nominal sampling rates from 0.8 kS/s to about 308 kS/s. Recorded mains tests confirm stable 50 Hz frequency readings at three settings. Collectively, these analyses establish the measurement capabilities and limitations of the proposed architecture while providing a framework for evaluating similar embedded instrumentation systems.

Ultimately, this work demonstrates that carefully designed microcontroller-based instrumentation can provide practical, portable, and affordable alternatives to commercial laboratory oscilloscopes for educational instruction, embedded systems experimentation, prototype development, and low-frequency electronic measurements.

Novelty of the Study

Unlike many existing low-cost oscilloscope implementations that focus primarily on hardware construction, this study links the firmware implementation directly to measured and theoretical performance. It shows that the effective resolution of the instrument is set by how the firmware reads the converter rather than by the converter itself, quantifies the sampling limits of each time-base setting, and validates the frequency measurement with recorded mains tests. The resulting framework is intended to help engineering educators and students evaluate and improve low-cost embedded oscilloscopes.

2 MATERIALS AND METHODS

2.1 Research Design

This study employed an engineering design and analytical performance evaluation approach. The work comprised four phases: (i) hardware design and construction, (ii) embedded firmware development, (iii) functional testing, and (iv) analytical evaluation of measurement performance. Phases (i) to (iii) were carried out in 2023, and the design records, firmware source code and test photographs were documented in the project report [9]. The prototype is no longer available for further testing. The analytical evaluation in this paper was therefore derived from the documented design, the firmware source code and the recorded test results.

The overall architecture is illustrated in Figure 1, which summarizes the signal acquisition, processing, display and power supply units of the oscilloscope.

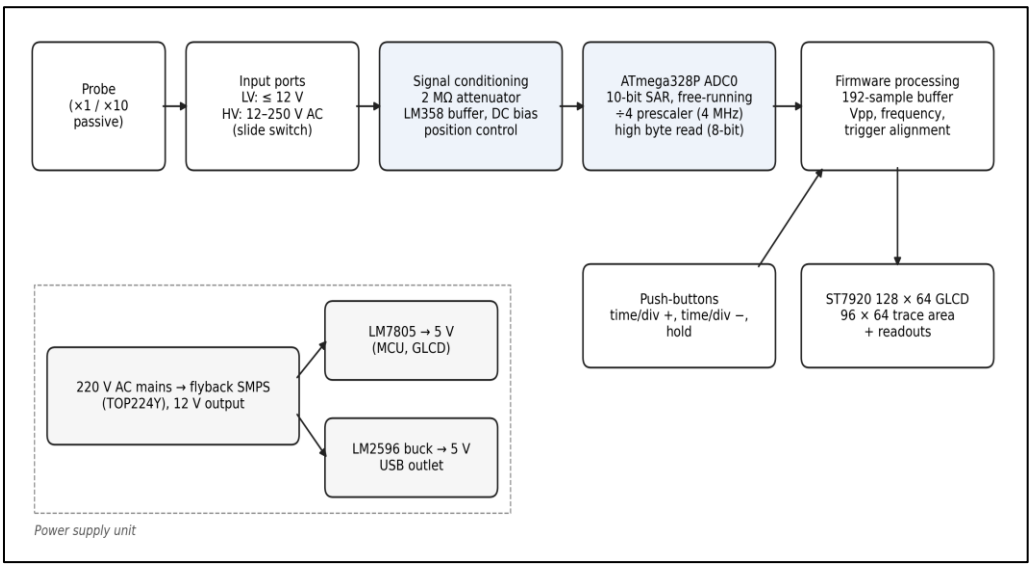


Figure 1: Block diagram of the ATmega328P-based digital oscilloscope showing the input, signal conditioning, acquisition, processing, display and power supply units.

2.2 System Architecture

The developed oscilloscope consists of five principal subsystems: signal acquisition unit; signal conditioning circuit; embedded processing unit; display subsystem; and user control interface.

The analogue input signal is first passed through an attenuation and conditioning network to ensure that the input voltage remains within the allowable operating range (0–5 V) of the ATmega328P ADC. The conditioned signal is converted by the internal ADC, of which the firmware retains the eight most significant bits, and transferred to the microcontroller for digital processing.

The embedded firmware reconstructs the sampled waveform, computes the peak-to-peak voltage and frequency, and renders the waveform on a 128 × 64 graphical liquid crystal display (GLCD). Three push-buttons provide user interaction: two increase and decrease the time base, and the third activates waveform hold. A slide switch selects the low-voltage or high-voltage input, and a potentiometer adjusts the vertical position of the trace.

2.3 Hardware Components

The oscilloscope hardware was designed using low-cost, commercially available electronic components to achieve affordability without significantly compromising measurement capability. The circuit was laid out in EAGLE CAD and fabricated in-house on an etched copper-clad board [9]. The principal hardware components are summarized in Table 1.

Table 1: Major hardware components of the oscilloscope.

Component	Specification	Function
Microcontroller	ATmega328P, 16 MHz	Signal acquisition and processing
ADC	Internal 10-bit SAR ADC; free-running; ÷4 prescaler; high byte read (8-bit)	Analogue-to-digital conversion
Display	128 × 64 ST7920 GLCD	Waveform and readout display
User controls	Three push-buttons; slide switch; potentiometer	Time base (+/−) and hold; input range; vertical position
Signal conditioning	2 MΩ resistive attenuator; LM358 operational amplifier; DC bias	Voltage scaling and level shifting
Probe	Passive probe, ×1/×10	Signal connection
Power supply	Flyback SMPS (TOP224Y); LM7805 regulator; LM2596 buck converter	5 V logic and display supply; 5 V USB output

SAR: successive approximation register; SMPS: switched-mode power supply.

The ATmega328P was selected because it integrates a 10-bit successive approximation ADC, programmable timers, interrupt controllers, serial communication interfaces, and sufficient memory resources required for embedded data acquisition applications [11, 12].

2.4 Signal Conditioning Circuit

Since the ADC accepts input voltages only within the range of 0–5 V, an analogue signal conditioning circuit was incorporated to scale the input signal while maintaining measurement fidelity. The instrument provides two input ports selected by a slide switch: a low-voltage port for signals of up to about 12 V and a high-voltage port for signals from about 12 V to 250 V AC [9].

The conditioning circuit consists of:

- A 2 MΩ resistive attenuation network on the high-voltage path;
- An LM358 operational amplifier stage that scales the attenuated signal to a maximum of 5 V;
- A DC bias that centres bipolar waveforms within the 0–5 V ADC range; and
- A potentiometer for vertical position adjustment.

The attenuation network scales higher input voltages into the measurable ADC range while preserving waveform characteristics. It allows mains-level voltages to be measured directly, without the external step-down transformer required by the earlier design [15].

2.5 Firmware Development

Embedded firmware was developed in C/C++ using the Arduino Integrated Development Environment (IDE). Graphical rendering was implemented using the U8glib graphics library [17, 18]. The firmware performs the following sequential operations: ADC initialization (AVcc reference, left-adjusted result, free-running mode, ÷4 prescaler); signal sampling (192 samples per acquisition); voltage calculation; frequency estimation; trace alignment and scaling; LCD rendering; key scanning; and continuous execution.

The firmware continuously repeats these operations to achieve real-time waveform display. The overall execution sequence is illustrated in Figure 2.

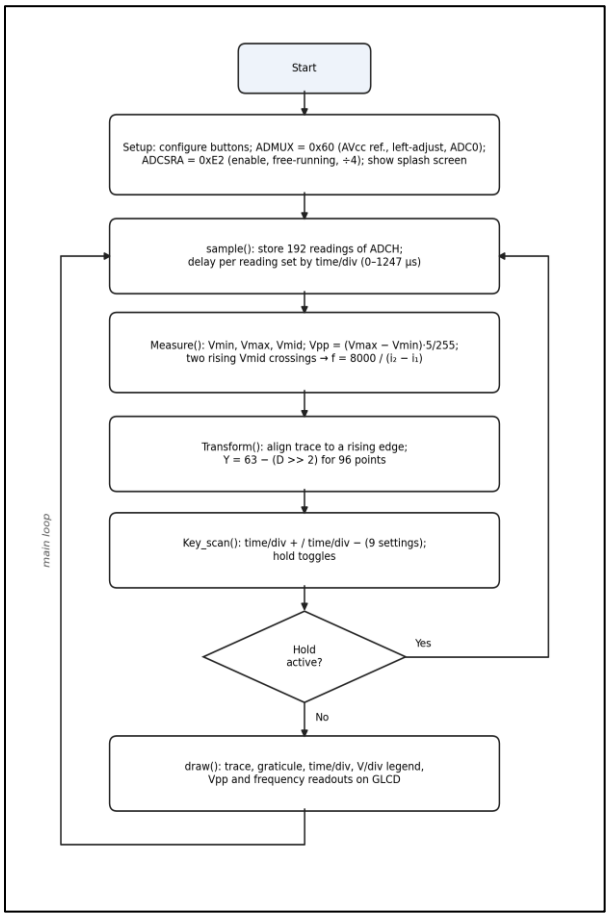


Figure 2: Firmware flowchart illustrating signal acquisition, processing, waveform rendering and user interaction.

2.6 Signal Sampling

The ADC is configured in free-running mode with a prescaler of 4, giving an ADC clock of 4 MHz from the 16 MHz system clock. Since one conversion takes 13 ADC clock cycles, the maximum conversion rate is [12]

$$f_{\mathrm{ADC,max}} = \frac{16\ \mathrm{MHz}}{4\times 13} \approx 307.7\ \mathrm{kS/s} \qquad (1)$$

During each acquisition, the firmware stores 192 readings in a buffer, inserting a software delay between readings that depends on the selected time-base setting. The display shows 96 samples across 12 horizontal divisions, that is, 8 samples per division. The nominal sampling rate for a time-base setting t_{div} is therefore

$$f_s = \frac{8}{t_{\mathrm{div}}} \quad (2)$$

Nine settings from 0.02 to 10 ms/div are available, corresponding to nominal sampling rates from 400 kS/s to 0.8 kS/s. At the fastest setting, the nominal rate exceeds the limit in Equation (1), so the effective rate is limited by the ADC. The 1 ms/div setting, with f_s = 8 kS/s, is the reference setting used by the frequency routine.

2.7 ADC Resolution Analysis

The minimum detectable voltage increment of the ADC is given by

$$\text{Resolution} = \frac{V_{\text{ref}}}{2^n} \quad (3)$$

where V_{ref} = 5 V and n is the number of bits used. Because the conversion result is left-adjusted and the firmware reads only the high byte (ADCH), n = 8. Substituting,

$$\text{Resolution} = \frac{5}{256} = 19.53 \text{ mV} \quad (4)$$

Therefore, each stored code corresponds to approximately 19.53 mV at the ADC input. If both result registers were read, n would be 10 and the resolution would be 4.88 mV.

2.8 Quantization Error

The theoretical quantization uncertainty associated with an ideal ADC is [8, 19]

$$Q_e = \pm\frac{\text{Resolution}}{2} = \pm 9.77 \text{ mV} \quad (5)$$

This value represents the inherent uncertainty introduced during analogue-to-digital conversion.

2.9 Nyquist Bandwidth

According to the Nyquist sampling theorem,

$$f_{\max} = \frac{f_s}{2} \quad (6)$$

At the reference setting (f_s = 8 kS/s), $f_{\max}$ = 4 kHz. At the fastest setting, the ADC limit of 307.7 kS/s gives $f_{\max} \approx 154$ kHz, and at the slowest setting (f_s = 0.8 kS/s) $f_{\max}$ = 400 Hz. Because a readable trace needs several samples per cycle, a practical display limit of about ten samples per period, $f_s/10$, was also evaluated.

2.10 Dynamic Range

The theoretical dynamic range of an ideal n-bit ADC is approximated by [8]

$$\text{DR} = 6.02n + 1.76 \text{ dB} \quad (7)$$

Substituting n = 8 yields

$$\text{DR} = 6.02(8) + 1.76 = 49.92 \text{ dB} \quad (8)$$

For the full 10-bit result, the same expression gives 61.96 dB.

2.11 Frequency Measurement

Signal frequency was estimated using midpoint-crossing detection. The firmware computes the midpoint of the minimum and maximum sample values, finds two consecutive rising crossings of this midpoint at sample indices i_1 and i_2, and calculates the frequency as

$$f = \frac{f_s}{i_2 - i_1} \quad (9)$$

The search windows limit a measurable period to at most about 96 samples, so the lowest measurable frequency at each setting is approximately $f_s/96$. Since the crossing positions are resolved to one sample, the relative resolution of the frequency reading is

$$\frac{\Delta f}{f} \approx \frac{1}{N} = \frac{f}{f_s} \quad (10)$$

where N is the number of samples per period.

2.12 Waveform Scaling

The stored 8-bit samples are transformed into LCD pixel coordinates before graphical rendering. Vertical scaling is performed according to

$$Y = 63 - \left\lfloor \frac{D}{4} \right\rfloor \qquad (11)$$

where D is the stored 8-bit sample (0–255) and 63 is the bottom pixel row of the 64-pixel trace area. Each pixel therefore represents four codes, or 78.1 mV at the ADC input. Horizontally, the trace is aligned to a rising edge of the waveform, and 96 samples are drawn across 96 pixels.

2.13 Functional Testing

The prototype was tested in 2023 using the 220 V, 50 Hz mains supply connected to the high-voltage port. Four tests were performed [9]: (i) waveform visualization with the mains input; (ii) frequency response, in which the frequency reading was observed as the time base was changed; (iii) a no-input test with the probe unconnected; and (iv) vertical position adjustment using the potentiometer. The displayed traces and readouts were photographed at several time-base settings. The frequency readings were compared with the nominal 50 Hz mains frequency and with the resolution predicted by Equation (10).

2.14 Performance Evaluation

The developed oscilloscope was evaluated using the following performance metrics: effective ADC voltage resolution; quantization uncertainty; dynamic range; sampling rate at each time-base setting; Nyquist and practical bandwidth; frequency measurement range and resolution; functional test results; and component cost.

These metrics were used to assess the suitability of the design for educational laboratories, embedded systems development, and low-frequency electronic measurements.

3 RESULTS

3.1 Performance Evaluation of the Developed Oscilloscope

The ATmega328P-based digital oscilloscope was evaluated using theoretical performance models, the firmware source code and the recorded functional tests. The evaluation focused on the principal performance indicators governing digital oscilloscope operation, namely effective resolution, quantization error, sampling rate, dynamic range, frequency measurement capability, and waveform display. These parameters collectively determine the measurement capability of embedded digital instrumentation and provide an objective basis for comparison with commercial digital storage oscilloscopes (DSOs).

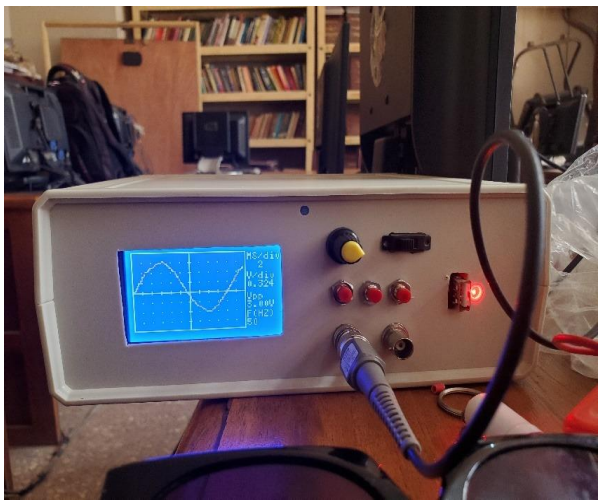


Figure 3: The completed oscilloscope prototype (2023), showing the GLCD, position control, input-range slide switch, push-buttons, USB outlet and probe input.

The completed prototype is shown in Figure 3. The oscilloscope provides nine time-base settings, with nominal sampling rates from 0.8 kS/s to about 308 kS/s. The corresponding Nyquist limits range from 400 Hz to about 154 kHz,

and the practical display bandwidth reaches about 30 kHz at the fastest setting. This range makes the instrument appropriate for mains-frequency measurements, audio-frequency signals, educational demonstrations, embedded systems debugging, and general-purpose low-frequency measurements.

The effective 8-bit data path provides a voltage resolution of 19.53 mV at the ADC input, with a quantization uncertainty of ±9.77 mV and a theoretical dynamic range of 49.9 dB. These values are adequate for visualizing waveforms and for low-frequency teaching measurements, although they are lower than the 10-bit hardware would allow.

3.2 ADC Resolution and Quantization Performance

With a reference voltage of 5 V and 8 bits retained, each stored code corresponds to 19.53 mV. The quantization uncertainty of ±9.77 mV represents 0.20% of the 5 V full-scale input, so digitization error contributes little to the overall uncertainty of waveform display under normal operating conditions.

The analysis also shows that the limiting factor is the firmware rather than the converter. Because the result is left-adjusted and only the high byte is read, the two least significant bits of the 10-bit conversion are discarded. Reading both result registers would improve the resolution to 4.88 mV and the quantization uncertainty to ±2.44 mV without any hardware change. On the display itself, the 64-pixel trace height gives 78.1 mV per pixel (Equation 11), so the display, rather than the ADC, limits the visible vertical detail.

The peak-to-peak voltage readout is calculated as $(D_{\max} - D_{\min}) \times 5/255$. Because this calculation is performed with integer arithmetic, the result is truncated to whole volts at the ADC input. This explains the constant readout of 3.00 V observed in the tests (Figure 4) and is a limitation of the current firmware rather than of the hardware.

These findings agree with the theoretical characteristics of successive approximation register (SAR) analogue-to-digital converters integrated within embedded microcontrollers and show that acceptable waveform display can be achieved without expensive external conversion hardware [8, 12].

3.3 Sampling Performance and Bandwidth Analysis

Sampling frequency remains the most significant factor governing oscilloscope performance. Table 2 lists the nominal sampling rate, Nyquist limit, practical display limit and lowest measurable frequency for each time-base setting, calculated from Equations (1), (2), (6) and (9).

Table 2: Sampling performance at each time-base setting.

Setting	Time base (ms/div)	Nominal f_s (kS/s)	Nyquist limit ($f_s/2$)	Practical limit ($f_s/10$)	Lowest measurable frequency ($f_s/96$)
1	0.02	400 (ADC-limited to ≈308)	≈154 kHz	≈30.8 kHz	≈3.2 kHz
2	0.05	160	80 kHz	16 kHz	1.67 kHz
3	0.1	80	40 kHz	8 kHz	833 Hz
4	0.2	40	20 kHz	4 kHz	417 Hz
5	0.5	16	8 kHz	1.6 kHz	167 Hz
6	1	8	4 kHz	800 Hz	83 Hz
7	2	4	2 kHz	400 Hz	42 Hz
8	5	1.6	800 Hz	160 Hz	17 Hz
9	10	0.8	400 Hz	80 Hz	8.3 Hz

Across the nine settings, the instrument covers frequencies from about 8 Hz to about 30 kHz with at least ten samples per period. Signals with components above the Nyquist limit of the selected setting cannot be reconstructed accurately and are expected to exhibit aliasing distortion. Consequently, the oscilloscope is intended primarily for: educational electronics laboratories; embedded systems development; sensor signal monitoring; mains-frequency and power electronics practical sessions; and low-frequency and audio-frequency analogue circuit analysis.

Because the sample interval is set by software delays rather than a hardware timer [20], the rates in Table 2 are nominal. Their accuracy is supported by the frequency tests in Section 3.5, in which three different settings produced the

expected 50 Hz reading. Although commercial digital oscilloscopes routinely operate at sampling frequencies ranging from several megasamples per second (MS/s) to several gigasamples per second (GS/s), such performance substantially increases system cost and power consumption. The design deliberately prioritizes affordability and portability while maintaining acceptable performance within its intended application domain.

3.4 Dynamic Range Evaluation

Dynamic range determines the ability of an oscilloscope to distinguish weak signals in the presence of stronger signals. Based on Equation (7), the dynamic range of the 8-bit data path is 49.92 dB. This value is comparable to that of entry-level commercial oscilloscopes with 8-bit converters and indicates satisfactory performance for educational laboratories and prototype measurements where extremely high precision is unnecessary.

Reading the full 10-bit result would raise the theoretical dynamic range to 61.96 dB. Higher-resolution oscilloscopes employing 12-bit, 14-bit, or 16-bit ADCs provide significantly greater dynamic range, but at considerably higher implementation cost. The present design therefore offers a reasonable compromise between measurement quality and affordability, with a clear, low-cost route to improvement.

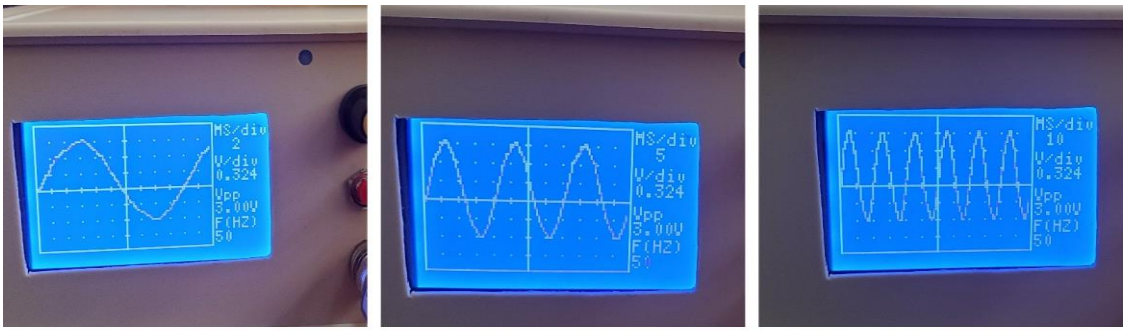
3.5 Frequency Measurement Performance

Frequency estimation was implemented using a midpoint-crossing detection algorithm within the firmware (Equation 9). For a 50 Hz signal, Equation (10) predicts the number of samples per period and the resulting resolution at each setting, as shown in Table 3. At 1 ms/div and faster settings, one period of a 50 Hz signal spans more than 96 samples, so the routine cannot find two crossings and no frequency is reported. A frequency reading therefore requires the time base to be set to 2 ms/div or slower.

This prediction agrees with the test report, which notes that the 50 Hz reading appeared only after the sampling setting was changed from its initial value [9]. The displays recorded at 2, 5 and 10 ms/div all reported 50 Hz (Figure 4), matching the nominal mains frequency within the resolution of each setting.

Table 3: Predicted and recorded frequency readings for the 220 V, 50 Hz mains input.

Time base (ms/div)	Nominal f_s (kS/s)	Samples per period, N	Predicted resolution ($1/N$)	Recorded reading
1	8	160	No reading (N > 96)	–
2	4	80	±1.25%	50 Hz
5	1.6	32	±3.1%	50 Hz
10	0.8	16	±6.25%	50 Hz



(a) 2 ms/div **(b) 5 ms/div** **(c) 10 ms/div**

Figure 4: Recorded displays for the 220 V, 50 Hz mains input at (a) 2 ms/div, (b) 5 ms/div and (c) 10 ms/div. Each display reports a frequency of 50 Hz and a peak-to-peak readout of 3.00 V.

The resolution improves as the signal occupies more samples per period, so the best frequency resolution is obtained at the fastest setting that still contains a full period within the 96-sample search window. Nevertheless, the achieved performance is adequate for educational measurements and embedded system diagnostics.

3.6 Waveform Reconstruction Capability

Waveform reconstruction constitutes one of the primary functions of a digital oscilloscope. The firmware converts the stored samples into graphical coordinates on the 128 × 64 GLCD, using a 96 × 64 pixel trace area with a graticule of 12 horizontal and 8 vertical divisions.

With the mains input, the prototype displayed stable sinusoidal traces at all recorded settings (Figure 4). The number of cycles shown agreed with the selected time base: about 1.2 cycles at 2 ms/div, 3 cycles at 5 ms/div and 6 cycles at 10 ms/div, which correspond to 24 ms, 60 ms and 120 ms across the 12 divisions. This agreement confirms that the time-base settings behave as designed.

The inclusion of nine time-base settings, waveform hold, input-range selection and vertical position adjustment improves usability by allowing users to inspect waveform characteristics under different measurement conditions. The volts-per-division legend is a fixed label in the firmware, and the vertical scale is not selectable in the present version.

3.7 Comparative Performance Analysis

To assess the practical capability of the instrument, its specifications were compared with those of a typical entry-level commercial digital storage oscilloscope. The comparison is presented in Table 4.

Table 4: Comparison between the developed oscilloscope and a typical commercial entry-level DSO.

Parameter	Developed Oscilloscope	Commercial Entry-Level DSO
ADC resolution	8-bit effective (10-bit hardware)	8–12 bit
Sampling rate	0.8 kS/s to ≈308 kS/s (9 settings)	1–100 MS/s or more
Bandwidth	≈30 kHz practical; 400 Hz–154 kHz Nyquist	20–100 MHz
Dynamic range	49.9 dB	50–74 dB
Maximum input	250 V AC, without external transformer	Depends on probe rating
Display	128 × 64 GLCD	High-resolution TFT/LCD
Portability	High	Moderate
Cost	₦51,810 (≈US$110, 2023)	More than ₦100,000 for a 50 kHz instrument (2023)
Intended application	Teaching, embedded systems, laboratory experiments	Professional engineering applications

TFT: thin-film transistor.

The comparison demonstrates that while commercial oscilloscopes significantly outperform the developed design in bandwidth and sampling speed, the developed instrument offers substantial advantages in affordability, portability, simplicity, and accessibility. These characteristics make it particularly suitable for educational institutions, developing laboratories, technical colleges, and embedded systems research environments.

3.8 Cost–Performance Analysis

One of the principal objectives of this study was to develop a practical oscilloscope using inexpensive and widely available electronic components. The total component cost of the prototype was ₦51,810 at 2023 prices, about US$110 at the May 2023 official exchange rate [9]. The largest items were the enclosure (₦18,000), the GLCD (₦9,500), the probe (₦8,000) and the microcontroller (₦4,500). All other items, including the power supply components, circuit board and etchant, amounted to ₦11,810.

The ATmega328P integrates the ADC, processing unit, timers, and communication peripherals within a single chip, thereby eliminating the need for dedicated signal-processing hardware. Similarly, the graphical LCD provides adequate waveform visualization while maintaining low power consumption and modest system complexity. The enclosure accounted for about a third of the total cost, so a simpler enclosure could reduce the cost further.

Consequently, the overall cost is well below that of commercial digital oscilloscopes while providing sufficient performance for instructional and low-frequency applications. This favourable cost-to-performance ratio makes the architecture particularly attractive for engineering education, laboratory demonstrations, and embedded instrumentation projects in resource-constrained environments.

4 DISCUSSION

The results demonstrate that the microcontroller-based oscilloscope balances performance, affordability, and implementation simplicity. Unlike many previously reported low-cost oscilloscope designs that emphasize hardware construction alone, the present study connects the firmware implementation to the resulting performance through quantitative models of resolution, sampling limits, quantization effects, dynamic range and frequency measurement [13, 14].

A key finding is that the effective resolution of the instrument is set by the firmware rather than by the hardware. The ATmega328P provides a 10-bit converter, but reading only the high byte reduces the resolution by a factor of four. Similarly, the whole-volt truncation of the peak-to-peak readout results from integer arithmetic in the firmware. Both limitations can be removed through firmware changes alone. This finding is relevant to educators and students, since many low-cost designs report the converter's nominal resolution rather than the resolution actually achieved by their firmware.

The frequency analysis also explains the behaviour observed during testing. The requirement for the period to fit within the 96-sample search window accounts for the absence of a frequency reading at faster settings, and the agreement of the 50 Hz readings at three settings supports the nominal sampling rates in Table 2.

Furthermore, the modular architecture provides a flexible platform for future enhancements, including timer-triggered sampling, full 10-bit acquisition, higher-speed microcontrollers, external high-resolution ADCs, Fast Fourier Transform (FFT) analysis, and wireless data transfer [16].

The results therefore demonstrate that affordable embedded digital oscilloscopes can significantly improve access to electronic measurement equipment in universities, technical institutions, and research laboratories, particularly within low-resource settings where acquisition of commercial laboratory instrumentation remains financially challenging [13, 14].

5 CONCLUSION

The present study designed, constructed and analytically evaluated a low-cost microcontroller-based digital oscilloscope capable of real-time visualization and measurement of low-frequency electrical signals. By integrating the ATmega328P microcontroller, signal conditioning circuitry, embedded firmware, a 128 × 64 graphical LCD and a switched-mode power supply, the system demonstrates that functional digital instrumentation can be implemented using inexpensive and readily available hardware components, at a component cost of ₦51,810 in 2023.

The analysis showed that the firmware retains eight bits of the 10-bit conversion, giving a voltage resolution of 19.53 mV, a quantization uncertainty of ±9.77 mV and a dynamic range of 49.9 dB. The nine time-base settings correspond to nominal sampling rates from 0.8 kS/s to about 308 kS/s, with Nyquist limits from 400 Hz to about 154 kHz and a practical display bandwidth of about 30 kHz.

Functional tests with the 220 V, 50 Hz mains supply produced stable sinusoidal traces and frequency readings of 50 Hz at the 2, 5 and 10 ms/div settings, in agreement with the predicted frequency resolution of 1.25% to 6.25%. The number of cycles displayed at each setting also agreed with the selected time base. These findings indicate that, despite its simple architecture, the instrument provides sufficient capability for instructional, prototyping, and troubleshooting applications where commercial oscilloscopes are unavailable or economically impractical.

This study also shows that the effective resolution of a low-cost oscilloscope can be limited more by its firmware than by its converter. Reading the full 10-bit result and using floating-point voltage calculation would improve the resolution to 4.88 mV and the dynamic range to 62 dB without any hardware change. The work therefore provides both a practical hardware implementation and a quantitative engineering analysis that can serve as a reference for future embedded instrumentation research.

Overall, the system demonstrates that affordable microcontroller-based digital oscilloscopes can substantially improve access to electronic measurement tools in educational institutions, developing laboratories, technical training centres, and low-resource engineering environments.

Practical Engineering Contributions

The present study makes several practical contributions to embedded instrumentation and engineering education.

- First, it demonstrates that a functional digital oscilloscope capable of measuring mains-level voltages directly can be built from inexpensive commercial off-the-shelf components for about US$110. This significantly reduces the financial barriers associated with laboratory instrumentation in developing countries.
- Second, the study provides an analytical framework that links firmware choices to resolution, sampling limits, dynamic range and frequency measurement. This framework can serve as a reference for future researchers designing similar embedded measurement systems.
- Third, the study identifies specific, low-cost firmware improvements, namely full 10-bit acquisition and floating-point voltage calculation, that would raise the performance of the existing hardware.
- Finally, the design supports practical engineering education by providing students with hands-on experience in analogue signal acquisition, embedded programming, printed circuit board (PCB) fabrication and electronic instrumentation.

Limitations of the Study

Despite its satisfactory performance, the oscilloscope has several limitations.

The firmware reads only eight bits of the 10-bit conversion, and the peak-to-peak voltage readout is truncated to whole volts at the ADC input. The readout is also not scaled by the input attenuation, so it does not directly give the voltage at the probe.

The sample interval is set by software delays rather than a hardware timer, so the sampling rates are nominal, and the firmware does not provide a selectable vertical scale or an adjustable trigger level. The practical bandwidth of about 30 kHz makes the instrument unsuitable for high-frequency radio-frequency (RF), communication, and advanced power electronics applications. The graphical LCD also offers limited display resolution compared with contemporary colour TFT displays used in commercial instruments.

Furthermore, experimental validation was limited to the 220 V, 50 Hz mains supply, and no simultaneous comparison with a commercial oscilloscope was recorded. The prototype is no longer available, so further tests could not be performed for this paper. Comprehensive experimental validation across a broader range of signal types, amplitudes and frequencies would further strengthen the assessment of the design.

Recommendations for Future Research

Based on the findings of this study, the following recommendations are proposed.

- The firmware should read the full 10-bit result and compute the peak-to-peak voltage in floating point, scaled by the input attenuation, to improve resolution and give the voltage at the probe directly.
- Sampling should be triggered by a hardware timer to make the sample interval deterministic and independent of software timing.
- Future versions should be validated against a calibrated commercial oscilloscope and signal generator using sine, square and triangular waveforms across the full frequency range, following recognized uncertainty guidelines.
- Higher-performance microcontrollers such as the STM32, ESP32 or RP2040, or external 12-bit high-speed ADCs, should be considered to increase sampling rate, resolution and bandwidth.
- Digital signal processing functions, including FFT analysis, digital filtering, automatic triggering and waveform averaging, should be incorporated to expand analytical capability.
- USB, Bluetooth or Wi-Fi interfaces should be added to support computer connectivity, data logging and remote laboratory applications.
- Automatic calibration routines should be implemented to compensate for offset errors, gain variations and component ageing.

STATEMENTS ON COMPLIANCE WITH ETHICAL STANDARDS

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Disclosure of conflict of interest

All authors declare that they have no financial or non-financial conflicts of interest.

Data Availability Statement

The firmware source code, design records, bill of materials and test photographs are documented in the 2023 project report [9] and are available from the corresponding author upon reasonable request.

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