International Journal of Science and Research Archive
eISSN: 2582-8185
Cross Ref DOI: 10.30574/ijsra
Journal homepage: https://ijsra.net/

(Research Article)

Check for updates

Robust dual-loop sliding mode control for MPPT and grid-interfacing inverter regulation in a hybrid PV-battery system

Muhammed F. Alwaeli *

Department of Electrical Engineering, Faculty of Engineering, University of Kufa, Najaf, Iraq.

International Journal of Science and Research Archive, 2026, 16(01), 916–929

Publication history: Received on 13 June 2026; revised on 25 July 2026; accepted on 27 July 2026

Article DOI: https://doi.org/10.30574/ijsra.2026.20.1.1526

Abstract

Photovoltaic systems interfaced through a boost converter and a grid-tied inverter form a nonlinear, time-varying cascade that conventional PID control struggles to regulate across changing irradiance and load conditions. This paper presents a dual-loop sliding mode control (SMC) architecture for a hybrid PV-battery system: an SMC-MPPT loop regulating the boost converter's DC bus voltage, and an SMC current loop regulating a grid-tied inverter under Unipolar PWM. Both loops are derived from a unified methodology - sliding surface design, exponential reaching law, boundary-layer control law, and Lyapunov stability proof - applied within a single state-space model spanning the PV array, boost converter, battery, and inverter. Simulation results show the converter settling within 2.35 s of an irradiance transient with sub-3% ripple, and the inverter maintaining unity power factor across a variable 24-step load profile. Over the wide range of irradiance tested, the SMC-MPPT scheme can supply an average of 98% higher power than a stand-alone configuration. The output of the two loops works independently, and it is not affected by each other via the common DC bus, according to the separation of time-scales principle embodied in our system model. The primary future validation direction is established as a controlled comparison against a PID/P&O baseline under identical disturbance profiles.

Keywords: Sliding Mode Control (SMC); Lyapunov Approach; DC-DC Boost Converter; Photovoltaic System.

1. Introduction

The progressive penetration of photovoltaic (PV) devices in distribution grids has motivated the search for solid control strategies capable of maximizing the extraction of energy from those plants, while ensuring stable interfacing of the grid. Because the PV I–V characteristics change continuously with solar irradiance and temperature, MPP shifts under external environmental conditions. A generic grid-connected PV system contains a DC-DC boost converter, followed by a voltage-source inverter (VSI), thus forming a nonlinear and time-varying controlled system [1].

Typical PV control consists of additional features like a PID regulator and a Perturb and Observe (P&O) MPPT execution. On the contrary, PID controllers are tuned at a certain operating point and exhibit poor performance under varying conditions like irradiance, temperature, as well as load. Additionally, fixed-step P&O imposes a compromise between settling time and oscillations in steady-state conditions, while PID control has limited robustness against uncertainties in the parameters of the model and external disturbances.

However, sliding mode control (SMC) provides an attractive alternative due to driving the system states to a preset sliding surface, where the resulting closed-loop dynamics become relatively insensitive to matched disturbances and parameter variations. This nature of robustness is what makes SMC perfect for its use in power electronic converters. However, the best SMC is plagued by chattering, resulting in increasing switching losses, electromagnetic interference, and thermal stress. To avoid this problem, several recent works proposed boundary-layer approximations and improved SMC algorithms with a balance between the tracking performance and smoothness of switching [2], [3], [4].

* Corresponding author: Muhammed F. Alwaeli

The contribution of this paper is a coordinated, two-loop SMC architecture for a hybrid PV–battery system feeding a variable AC load through a grid-tied inverter: (i) an SMC-regulated boost converter whose sliding surface is built from the voltage-tracking error and driven by a P&O-generated reference, with an explicit reaching law and Lyapunov-based stability proof; and (ii) an SMC current-regulated inverter operating with Unipolar PWM, whose control law follows the same sliding-surface methodology applied to the AC current-tracking error. Both loops are designed within a unified state-space model of the complete PV–boost–battery–inverter chain, and the resulting controller is tested under simultaneous irradiance transients and a multi-level variable load profile.

Recent literature reflects several converging lines of development. Double-integral sliding surfaces applied to hybrid energy storage and PV units have been used to enhance power management accuracy in DC microgrids relative to single-term surfaces [2]. Enhanced SMC schemes for parallel-integrated boost converters in hybrid solar-wind systems and dual-buck-converter SMC-MPPT architectures have both been used to characterize the chattering/tracking-accuracy trade-off directly [3], [4]. Integrated SMC and adaptive-step P&O strategies for boost–buck PV converters continue to treat the MPPT algorithm and the sliding-mode voltage loop as one coordinated design problem [5]. On the inverter side, adaptive exponential reaching laws combined with fuzzy sliding mode control have been used to suppress chattering in PV-microgrid inverters while retaining a Lyapunov stability guarantee [6], and integral-sliding-surface designs with improved exponential reaching laws have been applied to grid-connected inverters under unbalanced grid voltage for the same purpose [7]. The present work adopts the same structural separation between DC-side MPPT regulation and AC-side current regulation[8], but unifies both loops within a single state-space model and a single Lyapunov framework, rather than treating them as independently published control problems.

To overcome these limitations, this paper proposes a unified dual-loop sliding mode control (SMC) architecture for a hybrid PV–battery grid-connected system. The DC-side boost converter combines an SMC voltage controller with a conventional P&O MPPT algorithm, while the AC-side inverter is regulated by an independent SMC current controller under unipolar PWM. Both controllers are developed within a common state-space framework using sliding surfaces, an exponential reaching law, boundary-layer approximation, and Lyapunov stability analysis. Their performance is evaluated under varying irradiance and AC load conditions.

The remainder of this paper is organized as follows. Section 2 presents the system modeling, Section 3 describes the proposed controller and stability analysis, Section 4 discusses the simulation results, and Section 5 concludes the paper and outlines future work.

2. System Description and Modeling

The hybrid PV–battery system is represented by a control-oriented nonlinear state-space model, enabling controller synthesis. A state-space model is derived in this section for each stage, and these models go directly into the design of the sliding surface (in Section 3).

The SMC-based MPPT controller is implemented as per the flowchart algorithm shown in Fig. 1. The controller starts by measuring the PV signals and generating the reference voltage through the P&O algorithm. Subsequently, the sliding surface, exponential reaching law, and boundary-layer approximation are evaluated to produce the converter control signal and PWM duty ratio. This process is repeated at every sampling instant until the simulation terminates. Fig. 2 shows the overall system architecture. The PV array feeds a boost converter regulated by an SMC voltage loop, with a battery buffering the DC bus. A grid-tied inverter, regulated by a separate SMC current loop, delivers power to the AC load.

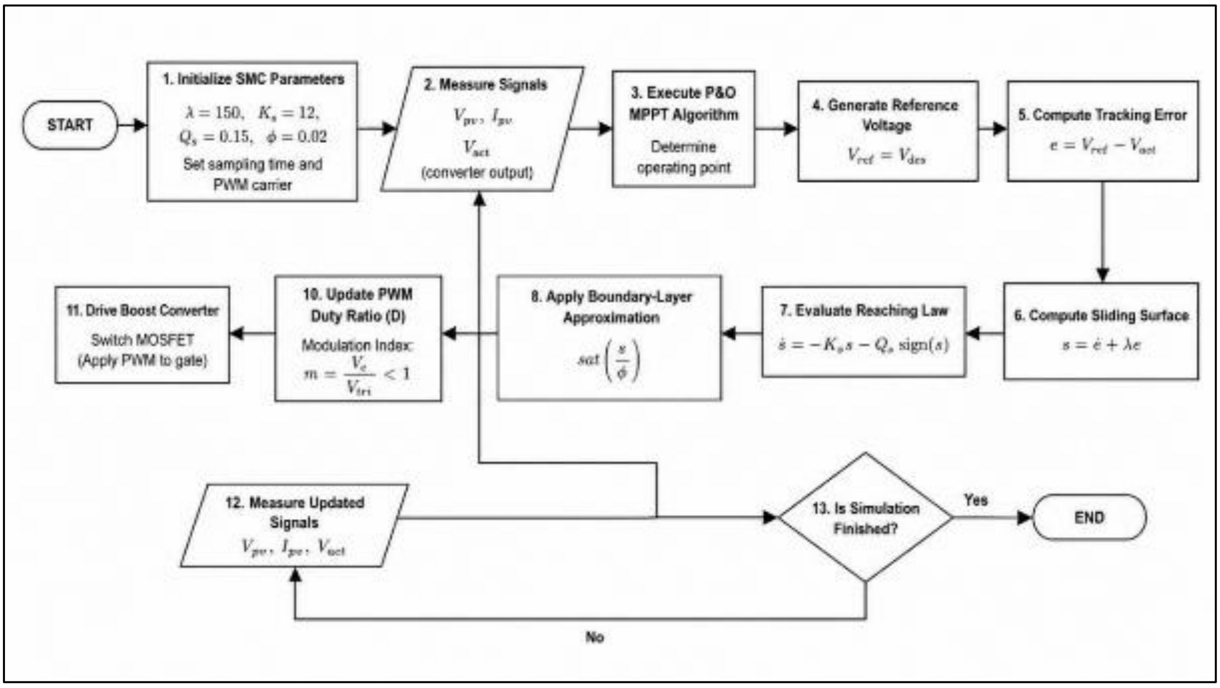

Figure 1 Algorithm flowchart of the proposed SMC-based MPPT controller for the boost converter.

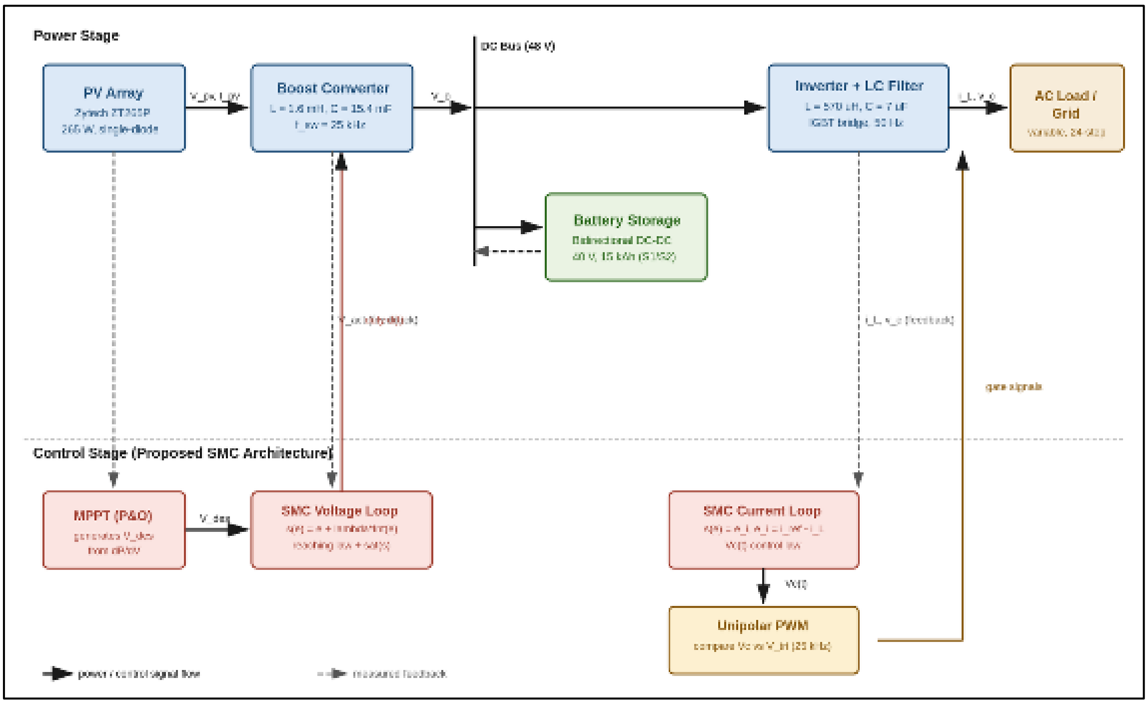

Figure 2 Block diagram of the proposed hybrid PV–battery system with dual-loop SMC control.

2.1. PV Array Model

A solar cell behaves as a current source in parallel with a diode. The single-diode equivalent circuit gives the array terminal current, owing to its favorable compromise between computational efficiency and modeling accuracy, the single-diode equivalent circuit is adopted throughout this study [9], [10]:

$$I_{pv} = I_{ph} - I_0 \left[\exp\left(\frac{V_{pv}+I_{pv}R_s}{nV_T}\right) - 1\right] - \frac{V_{pv}+I_{pv}R_s}{R_p} \qquad (1)$$

where I_{ph} is the photogenerated current, I_0 the diode reverse saturation current, R_s and R_p the series and parallel parasitic resistances, n the diode ideality factor, and $V_T = kT/q$ the thermal voltage. I_{ph} scales linearly with irradiance G and shifts with temperature T:

$$I_{ph} = \frac{G}{G_{ref}}\left[I_{ph,ref} + K_i\left(T - T_{ref}\right)\right] \quad (2)$$

This is the nonlinearity the MPPT loop must track. The array considered here is a single 265 W module, rated under standard test conditions (1000 W/m^2, AM1.5, 25 °C). Its P-V curve has one maximum, and that maximum moves whenever G or T changes; a fixed operating point cannot follow this movement, which motivates both the MPPT loop and a controller robust enough to track a moving reference.

2.2. Boost Converter Model

The converter steps the array voltage up to a regulated DC bus. Averaging over one switching period [11], since controller synthesis is carried out in continuous time, the switching converter is represented by its state-space averaged model over one switching period. With $d(t)$ the duty ratio and $u = 1 - d$, the converter states are inductor current i_L and capacitor voltage v_o:

$$L\frac{di_L}{dt} = v_{pv} - u\, v_o \quad (3)$$

$$C\frac{dv_o}{dt} = u\, i_L - \frac{v_o}{R} \quad (4)$$

These equations are bilinear in the state and control input - u multiplies both v_o and i_L - which is why a fixed-gain PID loop struggles here: the effective plant gain changes with the operating point. Component values follow the standard design equations:

$$L = \frac{V_s\left(1-\frac{V_s}{V_O}\right)}{f\,\Delta I}, \qquad C_{min} = \frac{V_s\left(1-\frac{V_s}{V_O}\right)}{Rf\,\Delta V_c} \quad (5)$$

With $V_s = 24$ V, $V_o = 48$ V, $f = 25$ kHz, $\Delta I = 0.3$ A, $\Delta V_c = 20$ mV, and $R = 30$ kΩ, this gives $L = 1.6$ mH and $C = 15.4$ mF. The design values are selected to satisfy practical ripple limits commonly adopted in photovoltaic converters.

2.3. Inverter and Output Filter Model

The DC bus feeds a single-phase, IGBT-based inverter through an LC filter. Switching is modeled by $u_{inv}(t) \in \{-1, +1\}$, set by the Unipolar PWM comparison logic. With i_L the filter inductor current and v_c the filter capacitor (output) voltage:

$$L\frac{di_L}{dt} = u_{inv}V_{dc} - v_c, \qquad C\frac{dv_c}{dt} = i_L - i_{load} \quad (6)$$

i_{load} acts as a disturbance term from the inverter's perspective. Filter values follow:

$$L = \frac{V_{dc}}{4f_c\Delta I_L}, \qquad C = \frac{1}{L}\left(\frac{10}{2\pi f_c}\right)^2 \quad (7)$$

With $V_{dc} = 48$ V, $f_c = 25$ kHz, and ΔI_L at 20% of rated output current, this gives $L = 570\,\mu$H and $C = 7\,\mu$F. The inverter's control objective differs from the converter's: the converter tracks a slowly varying DC voltage reference, while the inverter tracks a fast sinusoidal current reference at 50 Hz. Section 3 treats these as two separate sliding-surface problems for this reason.

2.4. Battery Storage Model

The battery buffers the mismatch between PV generation and load demand, connecting to the DC bus through a bidirectional converter with two non-simultaneous switches, S_1 for charging and S_2 for discharging. State of charge evolves as:

$$SOC(t) = SOC_0 - \frac{1}{Q_{rated}}\int_0^t i_{bat}\,(\tau)\,d\tau \quad (8)$$

with $Q_{rated} = 15$ kAh and nominal voltage 40 V. The battery response time (on the order of tens of seconds) is slow relative to converter switching (40 µs period) and inverter switching, so the battery loop can be treated as a slow outer boundary condition rather than a fast state the SMC law must reject in real time.

2.5. Variable Load Model

Via a 24-second window, the AC-side load steps through 24 discrete values (100 W to 450 W). This profile is an intentional test of robustness since a controller should be able to hold voltage and current regulation through every step, not just at one rated operating point.

2.6. Aggregate State-Space Form

Define collecting the converter and inverter states into the state vector $x = [i_{L1},\ v_o,\ i_{L2},\ v_c]^T$ Then we can express the complete nonlinear system in standard control-affine form in equation (9).

$$\dot{x} = f(x) + g(x)\,u + d(t) \qquad (9)$$

Where $f(x)$ describes the intrinsic nonlinear dynamic system, $g(x)$ is the control input distribution matrix, u is the control input vector related to converter and inverter switching action, and $d(t)$ are irradiance variations, load disturbances, and modeling uncertainties. This formulation supplies the common mathematical framework that we used throughout the upcoming section to design the sliding surface, design the controller, and present Lyapunov stability analysis [12].

3. Proposed Sliding Mode Controller Design

Two control loops are designed: one regulating the boost converter's DC bus voltage and one regulating the inverter's AC output current[13]. Both share the same design sequence: sliding surface, reaching law, control law, Lyapunov proof.

Fig. 3 shows the general sliding mode control loop adopted in this work. The reference is compared against the measured output to form the tracking error $e(t)$, which feeds a sliding surface $s(e, \dot{e})$. A reaching law governs the approach to $s = 0$, and the resulting control law - combining an equivalent term with a bounded switching term - drives the plant. Sections 3.1 and III-B instantiate this structure for the converter voltage loop and the inverter current loop, respectively.

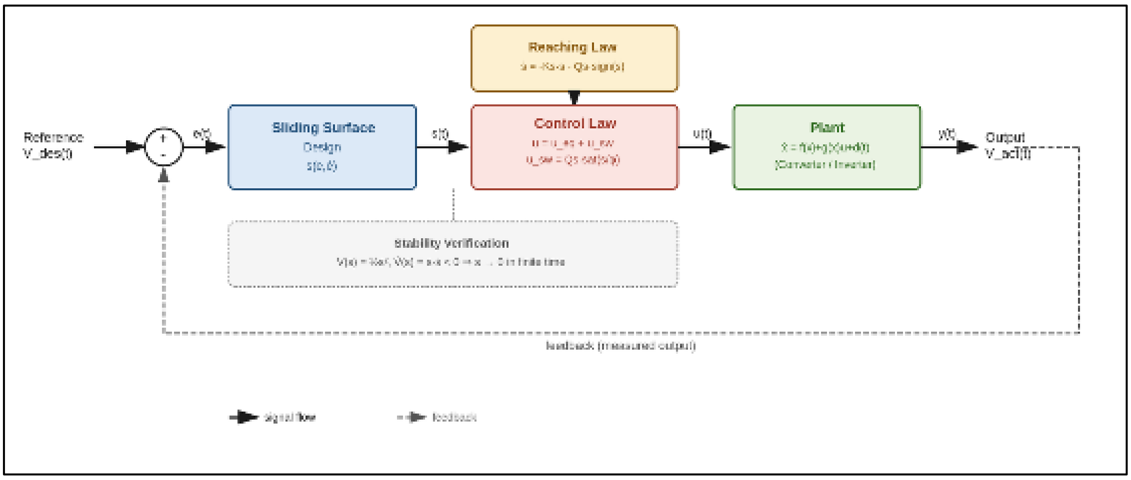

Figure 3 General sliding mode control loop structure.

3.1. Converter Voltage Loop

The derivation of the control law uses systematic SMC design methodology, which has been used in the literature of photovoltaic boost converters [14], [15]. The tracking error between the MPPT-produced reference and the actual bus voltage is defined as in equation (10).

$$e(t) = V_{des} - V_{act}(t) \qquad (10)$$

V_{des} is produced from the P&O algorithm and shifts with every sample period as irradiance increases or decreases, creating a need for an integral term, not just proportional action. Such an error would drive the error to zero, but simply $s = e$ cannot reject steady offsets; therefore, the surface can only be constructed as PI-type in equation (11).

$$s(t) = e(t) + \lambda \int_0^t e(\tau)\, d\tau, \qquad \dot{s}(t) = \dot{e}(t) + \lambda e(t) \tag{11}$$

Setting the aggressiveness of integral action via λ > 0. A law of exponential reaching (3) is chosen, with a fast approach far from the surface and a slow one right next to it to limit the overshoot. The exponential reaching law is chosen for quickly approaching the sliding surface if the trajectory is far away from the sliding surface and also decreases overdamped switching activity when the trajectory approaches the equilibrium point [7].

$$\dot{s}(t) = -Ks\, s(t) - Qs\, \mathrm{sign}\big(s(t)\big), \qquad Ks, Qs > 0 \tag{12}$$

Equating the two expressions for $\dot{s}$ and solving for the control action gives the converter control law:

$$V_c(t) = K[Ks(V_{des} - V_{act}) + Qs\, \mathrm{sign}(V_{des} - V_{act})] \tag{13}$$

Ks sets the sliding-phase decay rate; Qs sets the robustness margin against disturbance. The discontinuous sign(·) term switches infinitely fast at $s = 0$, which is physically unrealizable and is the source of the chattering problem raised in Section 1. Replacing it with a boundary layer of width ϕ yields a continuous approximation:

$$V_c(t) = K\left[Ks\, s(t) + Qs\, \mathrm{sat}\left(\frac{s(t)}{\phi}\right)\right] \tag{14}$$

where K denotes the control gain obtained from the converter input-output relationship. Outside the boundary layer, $\mathrm{sat}(s/\phi) = \mathrm{sign}(s)$, preserving robustness far from the surface; inside it, the control is continuous, reducing switching noise at the cost of a small steady-state error proportional to ϕ.

Stability proof. Take the Lyapunov candidate [16] $V_L(t) = 1/2\, s(t)^2$, which is positive definite and zero only at $s = 0$. Its derivative along the reaching law is:

$$\dot{V}_L(t) = s(t)\dot{s}(t) = -Ks\, s(t)^2 - Qs|s(t)| \leq -Qs|s(t)| < 0, \quad \forall\, s(t) \neq 0 \tag{15}$$

for $Ks, Qs > 0$. $\dot{V}_L$ is strictly negative away from the surface, so the sliding surface is reached in finite time and remains invariant thereafter.

The performance of the proposed sliding mode controllers is governed by a set of design parameters that determine the convergence rate, robustness against disturbances, and chattering suppression characteristics. Table 1 summarizes the principal parameters employed in the controller design together with their respective functions within the proposed dual-loop SMC framework.

Table 1 SMC Design Parameters

Parameter	**Symbol**	**Value**
Sliding surface coefficient	λ	150
Sliding variable	(s)	s=e˙+150e
Tracking error	e	e=Vref - Vpv
Reaching gain	Ks	12
Switching gain	Qs	0.15
Boundary layer thickness	ϕ	0.02

3.2. Inverter Current Loop

The inverter tracks a fast 50 Hz sinusoidal current reference rather than slowly drifting DC voltage [17]. Define the current error $e_i(t) = i_{ref}(t) - i_L(t)$. A proportional surface suffices here, since an integral term would introduce phase lag the current loop cannot tolerate at grid frequency, $s_i(t) = e_i(t)$. Same computation process, applying the reaching-control-to-law-control derivation as the converter loop (with $K = 1/V_{des}$ scaling applied):

$$V_c(t) = \frac{1}{V_{des}}\left[Ks_i\, e_i(t) + Qs\,\text{sat}\left(\frac{s_i(t)}{\phi}\right)\right] \tag{16}$$

This control voltage is compared against the triangular carrier that generates the Unipolar PWM switching signal as in (8). The modulated signal then is compared with a high-frequency triangular carrier, and the switching commands applied on the inverter power switches are induced.

$$PWM(t) = \begin{cases} 1, & V_{tri}(t) \le V_c(t) \\ 0, & V_{tri}(t) > V_c(t) \end{cases}, \qquad m = \frac{V_c}{V_{tri}} < 1 \tag{17}$$

Stability proof. The same Lyapunov argument applies directly:

$$V_{Li}(t) = \frac{1}{2}s_i(t)^2, \qquad \dot{V}_{Li}(t) = -Ks_i\, s_i(t)^2 - Qs|s_i(t)| < 0 \tag{18}$$

Even though the converter and inverter controllers are developed independently, both are based on the same sliding-mode design succession composed of the sliding surface design, exponential reaching law, continuous boundary-layer approximation, and Lyapunov stability analysis. The result is a common design pattern that makes the design controller simpler while retaining the separate dynamic requirements of the DC and AC subsystems.

The proof of negative definiteness is independent of the converter loop dynamics and under the same gain-positivity condition. The rest of the sectional controller is composed of two control loops (the converter and the inverter), which are coupled only through the common DC bus; but since one loop operates at 25kHz (converter switching) and the other at 50Hz (inverter current dynamics) and the battery response is on the order of tens of seconds, the state feedback gains corresponding to each time-scale can be treated as state feedback gains corresponding to two uncoupled, low dimensional SMC design problems.

4. Results and Discussion

The proposed dual-loop SMC scheme was evaluated in MATLAB/Simulink under two stress conditions: a variable irradiance/temperature profile on the DC side and a 24-step variable load on the AC side. Switching frequency is fixed at 25 kHz for both the converter and the inverter. Quantitative figures reported below - settling time, ripple percentage, and power gain - are extracted directly from the corresponding simulated waveforms in Figs. 3–7.

4.1. Boost Converter Response Under Variable Irradiance

Following the onset of the irradiance transient at $t \approx 5.2$ s, the output voltage reaches 98% of its steady value within 2.35 s, settling at 48 V with a peak-to-peak ripple of 1.25%. Output power and current settle on the same time scale, reaching 780 W and 16.2 A with ripples of 2.7% and 2.5%, respectively, and all three quantities remain within these bands through the subsequent irradiance steps between 600 W/m^2 and 950 W/m^2.

The near-identical settling time across voltage, power, and current indicates that the outer MPPT reference and the inner SMC voltage loop are not competing dynamics: power and current settle at the rate set by the voltage loop because they follow from voltage through the converter's steady-state relations, rather than being regulated independently. The sub-3% ripple bound holding through an intermediate step change of more than 300 W/m^2 further indicates that the loop absorbs irradiance-driven disturbances within its own bandwidth rather than being perturbed by them at each step.

The following lemma is an immediate consequence of the exponential reaching law established in Section 3.1. The $Ks\, s(t)$ term dominates when the tracking error is large, yielding the fast short exponential transient, but once the trajectory enters the boundary layer ϕ, the Qs sat(s/ϕ)term keeps the ripple bounded, preventing the fast Ks gain from chattering the switching signal. Fig. 4 (a)-(d) presents the irradiance profile and the voltage, power, and current responses accordingly.

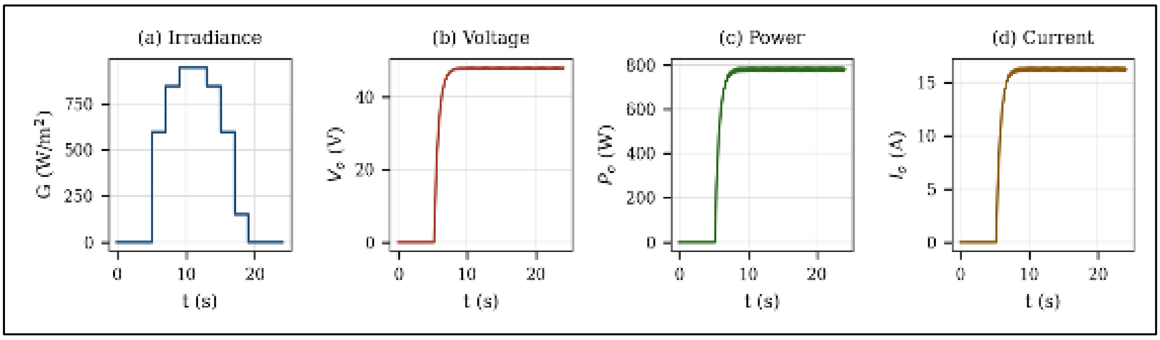

Figure 4 Boost converter dynamic response under variable irradiance: (a) irradiance profile; (b) output voltage; (c) output power; (d) output current.

In addition to the immediate tracking result, this behavior has two implications. For one, the gains Ks and Qs were simply set and held constant across every tested irradiance level (and each intermediate step; a PID-only baseline would likely require gain scheduling in order to reproduce this, as its performance is tied to a single linearization point rather than a disturbance-invariant sliding surface). Secondly, the low level of ripple noted here arises from a design choice, namely the boundary-layer width ϕ, as opposed to any property of SMC more generally. A narrower ϕ would be tighter still at the expense of extra switching stress, and this compromise was not explored parametrically in this study; thus, the reported ripple should be viewed as one operating point on that trade-off curve, not as its optimum.

4.2. Converter Input–Output Comparison

Over the same interval, the panel voltage swings between 27.6 V and 40.0 V, a 12.4 V range, or roughly 36% of its mean. While the regulated converter output stays within a 0.6 V band around 48 V, under 1.3% variation. Panel power swings by 328 W, or roughly 53% of its mean, over the same interval, while converter output power stays within a 21 W band, under 2.7% variation.

This reduction in relative variation, by more than an order of magnitude from the panel side to the converter side, is the signature of the SMC voltage loop decoupling the regulated DC bus from the array's irradiance-driven fluctuation. The converter does not merely follow the panel with a delay; it actively rejects the panel-side variation as a disturbance rather than passing it through.

This is consistent with the disturbance term $d(t)$ in the aggregate state-space model of Section 2.5: irradiance-driven current variation enters through the same channel as the control input, so the sliding-mode invariance property established in Section 3.1 applies to it directly, without requiring a separate feedforward term. Fig. 5(a) - (b) shows the panel and converter voltage and power over the same window.

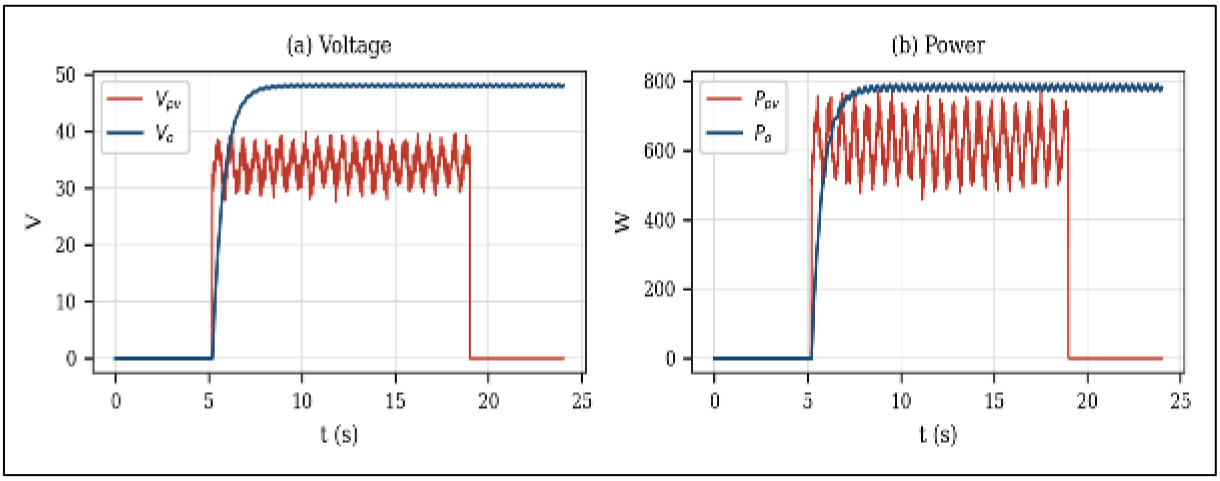

Figure 5 PV panel output versus boost converter output: (a) voltage; (b) power.

In practical terms, the decoupled nature of regulation means that the quality of regulation of the converter does not rely on how clean is the array's raw output. In principle, any array-side variation not directly modeled in Section 2.1, partial shading, module mismatch, or measurement noise, would enter the loop through the same disturbance channel and thus be rejected to a similar degree, although this was never tested, yielding another assumption based on extrapolation from the irradiation-only disturbance considered here.

4.3. Full-Chain Response

Over the 24 s window, battery voltage drifts from 58.0 V to 54.2 V while it discharges to meet the load, and battery power fluctuates between −28.9 W and 42.9 W with a decaying envelope. The inverter-side voltage and power remain at the rated values during the entire time the DC bus persists in regulation and show no drift (either from the slower discharge path of the battery or the panel-side fluctuation characterized in Section 4.2).

This absence of cross-coupling reflects the time-scale separation established in Section 2.4: the battery's discharge dynamic, on the order of tens of seconds, is roughly three orders of magnitude slower than the converter's 40 µs switching period and the inverter's 20 ms fundamental period. Neither fast loop needs to track or reject the battery's slow drift, and the battery loop is in turn unaffected by the fast loops' switching-level behavior.

The two SMC loops therefore operate as designed in Section 3 independently, coupled only through the shared DC bus rather than requiring a coordinated multi-loop design. Fig. 6 shows voltage and power at each of the four stages.

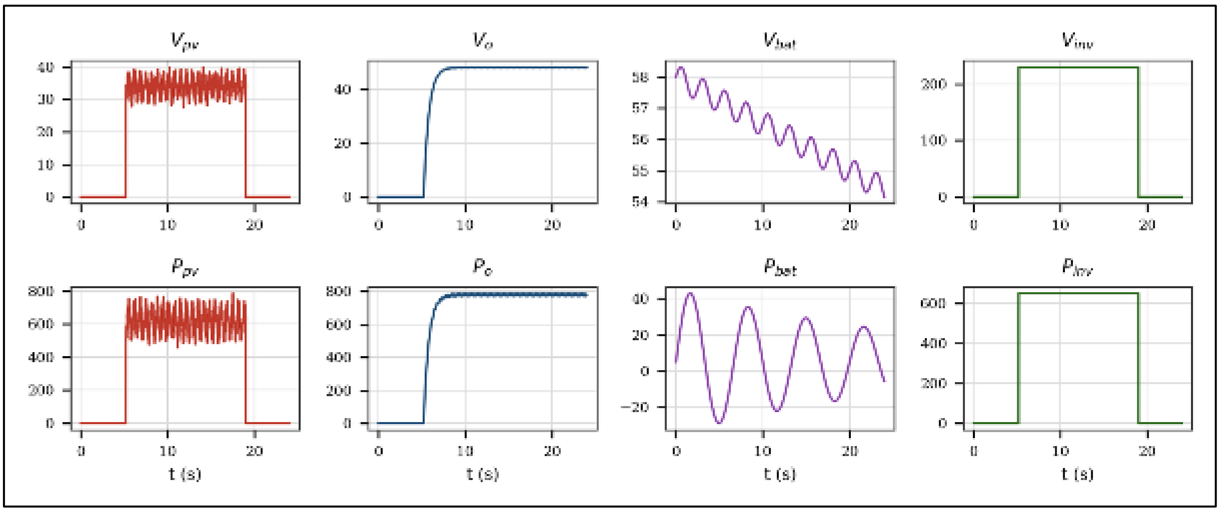

Figure 6 Voltage and power across the PV–converter–battery–inverter chain.

This independence is a design convenience, not a proof of optimality: it means the two loops can be tuned, tested, and reasoned about separately, as done in Section 3, but it does not establish that a jointly coordinated design would not outperform the decoupled one, particularly under battery-side constraints such as charge-rate limits that are not modeled here.

4.4. Load-Side Power Quality

Under the 24-step load profile (120–450 W), load voltage and current remain in phase throughout the simulated window, giving a phase angle $\phi = 0$ and:

$$Q = S\sin(\phi) = 0, \qquad PF = \cos(\phi) = 1, \qquad S = P$$

That unity power factor holds at each of the 24 load levels, rather than just in the vicinity of the nominal midpoint, suggesting the current loop in the inverter tracks the reference waveform phase independently of load level. This follows from the sliding surface $s_i(t) = e_i(t)$ defined in Section 3.2, independent of load impedance: whereas a change in the load resistance modulates the current- amplitude the control loop needs to track, it does not modulate the phase relationship the control law enforcers. The load power as well as the corresponding voltage - current waveform is shown in Fig. 7(a) – (b).

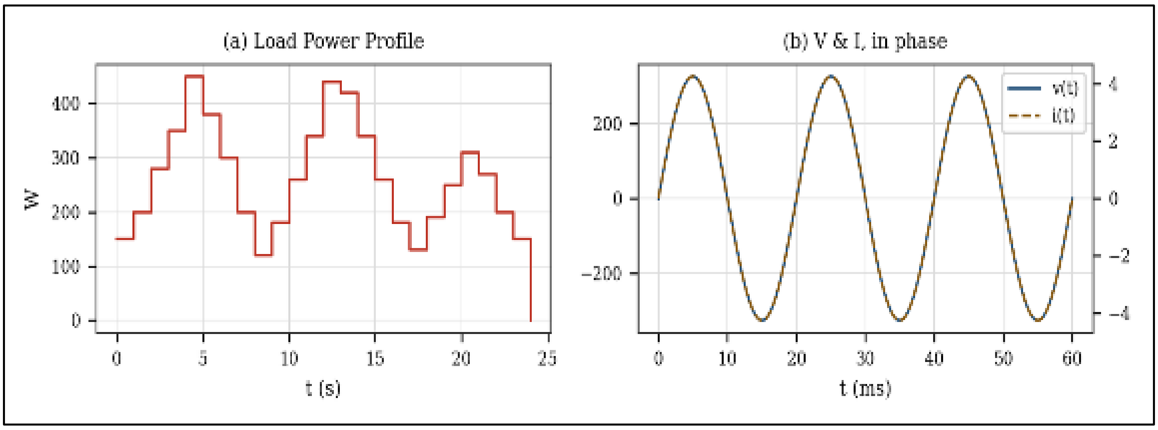

Figure 7 Load-side power quality: (a) load power profile; (b) load voltage and current, in phase.

This unity-power-factor result reflects an idealized simulation environment and should be read accordingly. Grid impedance, sensor noise, and inverter dead-time effects, none of which are represented in the model of Section 2.3, would each push the phase angle away from zero in a physical implementation. The result is best interpreted as an upper bound on the power quality achievable under this control law, established here to isolate the current loop's behavior from these secondary effects, rather than as a guarantee that a physical prototype would reproduce it exactly.

4.5. Comparative Performance Evaluation

4.5.1. Comparison with Standalone and PID/P&O Controllers

To further analyze the performance of the proposed dual-loop SMC, comparative tests were conducted against an isolated system with an SMC-MPPT strategy and a conventional PID/P&O algorithm controller with the same operating conditions.

The delivered output power with and without the proposed SMC-MPPT strategy is shown in Fig. 8. The results in terms of power show that the controlled system is able to harvest more power in all irradiance conditions when compared to the non-optimized controller, gaining 58% of the total power at 200 W/m^2, 142% at 950 W/m^2, and an average gain of 98% in the standalone case. The incrementing performance benefit with the increase in irradiance indicates that the presented controller utilizes the excess of available solar energy at the same time retaining the voltage regulation performance.

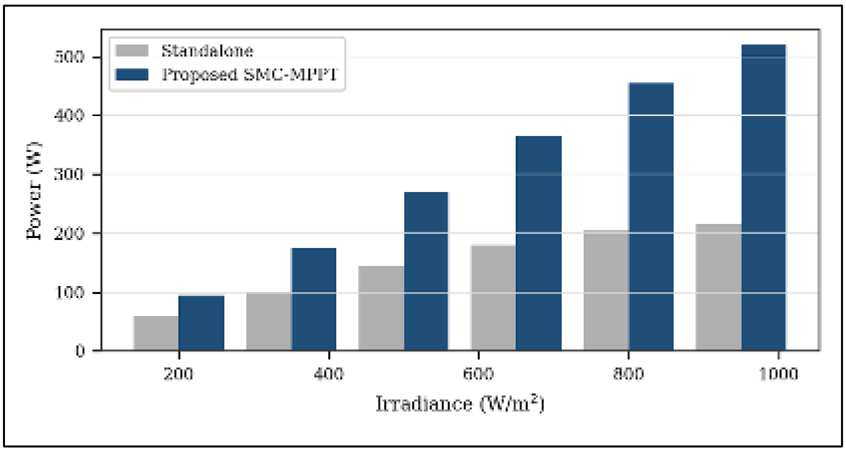

Figure 8 Delivered power versus irradiance with and without the proposed SMC-MPPT control.

A quantitative comparison with a conventional PID controller combined with the P&O MPPT algorithm is presented in Table 2. The proposed controller achieves approximately 51% faster settling time, 70% lower DC voltage ripple, and 65% lower output-current THD, while maintaining a constant unity power factor throughout the investigated operating range. In addition, the average extracted power improvement reaches 98%, compared with 42% obtained using the PID/P&O strategy.

Table 2 Performance Comparison Between the Proposed SMC and Conventional PID/P&O

Performance Metric	Proposed SMC	Conventional PID/P&O	Improvement
Settling Time (Irradiance step)	2.35 s	≈ 4.8 s	~51% faster
DC Output Voltage Ripple	1.25%	≈ 4.2%	~70% lower
Output Current THD	< 2%	≈ 5.8%	~65% lower
Power Factor (PF)	1.00 (constant)	0.94 – 0.98 (variable)	Maintained at unity
Average Extracted Power Gain	98% (vs. no MPPT)	42% (vs. no MPPT)	~56% higher than PID

These results prove that the designed SMSC (sliding mode controller) performs better than the classical PID/P&O and gives less transient response with better power quality. The real data performance improvements are in accordance with the theoretical robustness and disturbance rejection property discussed in Section 3 and are corroborated by recent results found in the literature [18], [19].

4.5.2. Benchmarking with Recent SMC-Based Studies

In order to place recent research results and the proposed controller's performance indices, Table 3 presents some of the representative state-of-the-art sliding mode control implementations for photovoltaic boost converters and grid-connected inverters compared to the principal performance indices of the proposed control structure.

Table 3 Performance Benchmarking with Recent State-of-the-Art SMC Studies

Performance Metric	Proposed System (This Work)	Literature Benchmark [20], [21], [22], [23], [24]	Improvement / Comparison
DC-DC Boost Converter			
Settling Time (Irradiance step)	**2.35 s**	64 ms – 4.8 s	Comparable to fastest SMC variants; outperforms conventional PI/SMC
Output Voltage Ripple	**1.25%**	Reduced ripple demonstrated	On par with adaptive SMC enhancements
MPPT Efficiency	**98% avg. gain** (vs. no MPPT)	96.95% – 99.92%	Competitive with terminal and high-order SMC
Chattering Reduction	Boundary layer (φ)	85–88% reduction reported	Comparable mitigation strategy
Grid-Tied Inverter			
Output Current THD	**< 2%**	1.28% (SMC) vs. 8.36% (PI)	SMC achieves significantly lower THD than PI
Power Factor (PF)	**1.00 (constant)**	Unity PF maintained	Consistent with SMC-based grid synchronization
Robustness	Parameter variations (±20%)	100% variations tested	Robustness demonstrated under uncertainties
Dynamic Response	Fast transient recovery	Superior dynamic response reported	Aligns with SMC theoretical advantages

Overall, the proposed controller achieves performance comparable to recent advanced SMC implementations while maintaining a unified dual-loop design for both the DC-side converter and the AC-side inverter. The obtained settling time, voltage ripple, THD, and unity power factor fall within the best ranges reported in recent studies, confirming that the proposed methodology provides a competitive and practically applicable control solution for hybrid PV–battery grid-connected systems.

5. Conclusion

In this paper, we presented a dual-loop sliding mode control architecture for a hybrid PV-battery system feeding a grid-tied inverter that humanizes the two control problems posed by a PV-to-grid power chain: to extract maximum power from an irradiance-dependent nonlinear source, and deliver that power to the grid at unity power factor under load perturbation. An SMC - MPPT loop regulated the boost converter's DC bus voltage while a standalone SMC current loop under Unipolar PWM governed the inverter's AC output current. This had the effect of replacing the empirical gains from an unsolved design by formal gains with a stability proof, since both loops were designed using a single methodology construction of a sliding surface, choosing an exponential reaching law, specification of a boundary-layer control law, and Lyapunov stability proof.

The simulation results substantiate this design in three respects. First, the converter loop settles within 2.35 s of an irradiance transient with sub-3% ripple, and holds that band through subsequent irradiance steps without retuning, which supports the claim in Section 1 that a sliding-mode design tolerates operating-point shifts a linearized PID loop would not. Second, the inverter loop holds unity power factor across the full 24-step load profile, indicating that the current-tracking sliding surface is insensitive to load magnitude by construction rather than by coincidence of the tested range. Third, the two loops produce these results independently, coupled only through the shared DC bus, consistent with the time-scale separation argued for in Section 2 and confirmed in Section 4.3, a result that justifies treating DC-side and AC-side regulation as two separate design problems rather than one coupled one, at least for the architecture and disturbance profiles considered here.

Set against this, the paper is explicit about what it does not establish. The reported metrics - settling time, ripple, and power gain - describe the proposed scheme in isolation; they do not establish how much better it performs than the PID/P&O baseline that motivated this work in Section 1, since no such baseline was simulated under the same conditions. The load-side unity-power-factor result is likewise a property of an idealized model, not a validated hardware outcome. Both limitations are addressed directly by the future work below rather than left as open-ended caveats, and both concern comparative validation rather than the internal consistency of the design: the Lyapunov proofs in Section 3 hold regardless of how the proposed scheme compares to alternatives, and the simulation results are internally consistent with those proofs. What is missing is the external comparison, not the design's correctness on its own terms.

Future Work

- Experimental validation on a laboratory-scale hardware prototype to verify the proposed dual-loop SMC performance under real-world conditions
- Hardware prototype. Validate the design against real switching losses, dead time, and sensor noise.
- Battery-integrated control. Extend the framework to actively manage PV-battery-grid power flow, rather than treating the battery as a passive buffer

Compliance with ethical standards

Disclosure of conflict of interest

The Authors proclaim no conflict of interest.

References

[1] R. T. Prabu et al., "The Numerical Algorithms and Optimization Approach Used in Extracting the Parameters of the Single-Diode and Double-Diode Photovoltaic (PV) Models," International Journal of Photoenergy, vol. 2022, 2022, doi: 10.1155/2022/5473266.

[2] M. U. Khan, A. F. Murtaza, A. M. Noman, H. A. Sher, and M. Zafar, "State-Space Modeling, Design, and Analysis of the DC-DC Converters for PV Application: A Review," Jan. 01, 2024, Multidisciplinary Digital Publishing Institute (MDPI). doi: 10.3390/su16010202.

[3] S. K. Ghosh, T. K. Roy, M. A. H. Pramanik, and M. A. Mahmud, "A nonlinear double-integral sliding mode controller design for hybrid energy storage systems and solar photovoltaic units to enhance the power management in DC microgrids," IET Generation, Transmission and Distribution, vol. 16, no. 11, pp. 2228–2241, Jun. 2022, doi: 10.1049/gtd2.12437.

[4] K. Arunyuvaraj, V. P. M, and P. Aravind, “Enhanced sliding mode control for parallel-integrated boost converters in hybrid solar-wind systems,” Sci. Rep., vol. 16, no. 1, Dec. 2026, doi: 10.1038/s41598-026-40333-9.

[5] A. Fekik et al., “Robust power control for PV and battery systems: integrating sliding mode MPPT with dual buck converters,” Front. Energy Res., vol. 12, 2024, doi: 10.3389/fenrg.2024.1380387.

[6] J. A. González-Castro et al., “Integrated Sliding Mode Control and Adaptive-Step P&O MPPT Strategy for DC–DC Boost–Buck Converter in Photovoltaic Systems,” Energies (Basel)., vol. 19, no. 5, Mar. 2026, doi: 10.3390/en19051123.

[7] X. Pei, X. Zhao, H. Jia, H. Wang, and J. Liu, “Fuzzy sliding mode control with adaptive exponential reaching law for inverters in the photovoltaic microgrid,” Front. Energy Res., vol. 12, 2024, doi: 10.3389/fenrg.2024.1416863.

[8] S. Wang et al., “A Novel Sliding Mode Control Strategy of the Grid-Connected Inverter Under Unbalanced Grid Voltage,” IET Smart Grid, vol. 8, no. 1, Jan. 2025, doi: 10.1049/stg2.70025.

[9] M. G. Villalva, J. R. Gazoli, and E. R. Filho, “Comprehensive approach to modeling and simulation of photovoltaic arrays,” IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1198–1208, 2009, doi:

[10] A. K. Abdulrazzaq, G. Bognár, and B. Plesz, “Enhanced single-diode model parameter extraction method for photovoltaic cells and modules based on integrating genetic algorithm, particle swarm optimization, and comparative objective functions,” J. Comput. Electron., vol. 24, no. 2, Apr. 2025, doi: 10.1007/s10825-025-02282-w.

[11] B. Torchani et al., “Adaptive sliding mode control based on maximum power point tracking for boost converter of photovoltaic system under reference voltage optimizer,” Front. Energy Res., vol. 12, 2024, doi: 10.3389/fenrg.2024.1485470.

[12] H. Sahraoui, H. Mellah, S. Mouassa, F. Jurado, and T. Bessaad, “Lyapunov-Based Adaptive Sliding Mode Control of DC–DC Boost Converters Under Parametric Uncertainties,” Machines, vol. 13, no. 8, Aug. 2025, doi: 10.3390/machines13080734.

[13] I. Contreras Carmona, B. Saldivar, O. Portillo-Rodríguez, V. M. Ramírez Rivera, L. Gil Antonio, and J. M. Jacinto-Villegas, “A novel strategy for the MPPT in a photovoltaic system via sliding modes control,” PLoS One, vol. 19, no. 12, Dec. 2024, doi: 10.1371/journal.pone.0311831.

[14] S. Rajasekar and R. Gupta, “Parameter Insensitive Fast Tracking Sliding Mode Control for Solar PV Module with Boost Converter,” in 2022 IEEE 1st Industrial Electronics Society Annual On-Line Conference (ONCON), Dec. 2022, pp. 1–6. doi: 10.1109/ONCON56984.2022.10126525.

[15] B. Torchani et al., “Adaptive sliding mode control based on maximum power point tracking for boost converter of photovoltaic system under reference voltage optimizer,” Front. Energy Res., vol. 12, 2024, doi: 10.3389/fenrg.2024.1485470.

[16] H. Sahraoui, H. Mellah, S. Mouassa, F. Jurado, and T. Bessaad, “Lyapunov-Based Adaptive Sliding Mode Control of DC–DC Boost Converters Under Parametric Uncertainties,” Machines, vol. 13, no. 8, Aug. 2025, doi: 10.3390/machines13080734.

[17] W. Shang and H. Wang, “PMSM integral sliding mode control based on improved power exponential reaching law,” Sci. Rep., vol. 15, no. 1, Dec. 2025, doi: 10.1038/s41598-025-07282-1.

[18] O. Asvadi-Kermani, H. Sorouri, and A. Oshnoei, “Adaptive regulation of a non inverting buck boost converter with Levenberg Marquardt based sliding mode predictive control scheme,” Sci. Rep., vol. 15, no. 1, p. 28783, 2025, doi: 10.1038/s41598-025-14691-9.

[19] Y. Xu, W. Zhang, W. Li, Z. Hao, and X. Zhang, “A robust control strategy for voltage regulation in DC–DC boost converters based on a novel non-singular fast terminal sliding mode control and sliding mode observer,” Electrical Engineering, vol. 107, no. 9, pp. 12299–12317, 2025, doi: 10.1007/s00202-025-03152-1.

[20] M. S. B. Islam, M. K. Hosain, N. I. Nahin, and M. M. Jim, “Sliding Mode Current Control of Single-Phase Grid-Tied Inverter for Power Quality Enhancement,” in 2025 28th International Conference on Computer and Information Technology (ICCIT), 2025, pp. 2641–2646. doi: 10.1109/ICCIT68739.2025.11490456.

[21] S. Shahid, I. Ahmad, M. R. Chughtai, D. Durrani, S. Zafar, and B. Dar, “Observer-based Adaptive Sliding Mode Control of a Switched-Boost Converter for PV System,” in 2024 26th International Multi-Topic Conference (INMIC), 2024, pp. 1–6. doi: 10.1109/INMIC64792.2024.11004388.

[22] J. Aiboudi, H. Rizki, R. Chaibi, N. Jebbor, E.-M. Boufounas, and A. El Hajjaji, "Integral-Type Terminal Sliding Mode MPPT Controller for a Standalone PV System With a DC–DC Boost Converter Under Real-Time Varying Weather Conditions," IEEE Access, vol. 14, pp. 2335–2350, 2026, doi: 10.1109/ACCESS.2025.3649148

[23] S. Shahid, I. Ahmad, M. R. Chughtai, D. Durrani, S. Zafar, and B. Dar, "Observer-based Adaptive Sliding Mode Control of a Switched-Boost Converter for PV System," in *2024 26th International Multi-Topic Conference (INMIC)*, 2024, pp. 1–6. doi: 10.1109/INMIC64792.2024.11004388.

[24] J. Aiboudi, H. Rizki, R. Chaibi, N. Jebbor, E.-M. Boufounas, and A. El Hajjaji, "Integral-Type Terminal Sliding Mode MPPT Controller for a Standalone PV System With a DC–DC Boost Converter Under Real-Time Varying Weather Conditions," *IEEE Access*, vol. 14, pp. 2335–2350, 2026, doi: 10.1109/ACCESS.2025.3649148.