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SAIF-Guided In-Design IR Analysis with PnR: A Unified Flow for Power-Aware SoC Implementation

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Abstract

As new System-on-Chip (SoC) architectures continue to emerge at an accelerated rate, the need for efficient power management strategies has become imperative. The high functionality requirements combined with strict power consumption controls are essential in modern applications such as mobile computing, automotive electronics, and Internet-of-Things (IoT) systems. This paper reviews the implementation of SAIF-guided in-design IR analysis as part of the physical design process, serving as a logical extension of power-aware SoC implementation in Place-and-Route (PnR). By incorporating Switching Activity Interchange Format (SAIF) data earlier in the design cycle, designers can resolve IR drop problems more efficiently, leading to improved power integrity and enhanced chip reliability. The paper presents findings from recent work on dynamic mapping heuristics, voltage/frequency scaling, RTL-level optimization, and hybrid prediction models. It therefore provides a comprehensive discussion of power optimization techniques that leverage integrated modeling, validation methods, and predictive techniques. The combination of traditional and intelligent solutions in integrating power concerns into advanced SoC-based systems is demonstrated through UVM-based verification, machine learning-based power estimation, and clock-gating technology integration.

Keywords: Power-aware design; System-on-Chip; SAIF-guided analysis; In-design IR drop

1. Introduction

The continued scaling of semiconductor technologies has made it possible to place billions of transistors on a single System-on-Chip (SoC). Although this has led to an incredible increase in processing power, it has also introduced numerous design challenges, most notably issues related to power integrity and power efficiency. The importance of power-sensitive design practices has increased significantly due to sustainability concerns, battery-powered devices, and thermal constraints.

Traditional design flows treated power estimation and integrity analysis as post-layout concerns. However, late intervention often leads to inefficient and potentially risky fixes, as well as expensive design re-spins. To reduce these risks, existing methodologies are shifting toward in-design IR analysis, where Switching Activity Interchange Format (SAIF) files are utilized to implement power profiling during the Place-and-Route (PnR) stage. This paper reviews this integrated flow and evaluates the effectiveness of implementing SAIF-informed data in the early stages of design to improve power management, particularly in mitigating voltage drops (IR drop).

Power analysis can be generated using the switching activity of RTL signals recorded in SAIF files with high accuracy, and this information can be utilized in physical design flows. This is necessary because IR drop—the voltage loss over resistive paths in the power distribution network—can cause timing violations, functional faults, and device degradation. A coherent flow that integrates both IR analysis and PnR enables designers to identify hotspots early in

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the design stages, implement corrective measures such as strengthening power grids or cell spreading, and ensure that the SoC meets power integrity requirements without compromising performance or area.

2. Unified Model-Based Approaches for Power-Aware Mapping

Power-sensitive dynamic mapping heuristics can significantly reduce energy consumption in NoC-based multiprocessor SoCs (MPSoCs). When implemented jointly as models, they enable runtime flexibility in task deployment, considering not only computational load but also the power characteristics of individual cores and communication links. In this way, power is conserved without negatively impacting throughput or latency. This approach aligns well with the SAIF-based methodology, as it models fine-grained activity between processing elements and routers [1].

The framework model is based on energy-conscious decision-making using SAIF traces generated during functional simulation. The use of activity data in mapping decisions allows chip regions with high switching activity to be dynamically identified and balanced so that power peaks are minimized and IR stability is enhanced. In contrast to static methods, dynamic heuristics reassign task mappings at runtime based on evolving workload and temperature variations, directly responding to energy hotspots and preventing incremental overload of the power delivery system.

Moreover, adaptive frequency and voltage scaling mechanisms can be implemented alongside complex power-state transition modeling without conflicting with task scheduling. The interaction between SAIF-based input heuristics and NoC mapping heuristics exemplifies how simulation-based metrics can enable power-conscious system adaptation.

3. Power-Aware Verification Using Dynamic Voltage and Frequency Scaling (DVFS)

Verification has traditionally been a bottleneck in SoC design, particularly for power-aware validation. UVM-based approaches have been developed to support power domain testing, especially for dynamic voltage and frequency scaling (DVFS). This is particularly important as power management units increasingly implement aggressive DVFS policies to minimize power consumption without reducing performance. In this context, SAIF files are essential, as they enable simulation tools to estimate power transitions under realistic workloads [2].

DVFS verification involves simulating various voltage and frequency conditions within a testbench environment, allowing the design to be evaluated under different power levels. When combined with SAIF-based activity modeling, signal transitions can be accurately represented, ensuring that transitions operate correctly and remain power-safe with respect to power integrity. This prevents situations where increasing frequency temporarily raises power consumption beyond what the voltage regulator can handle, potentially causing logic failures or data corruption.

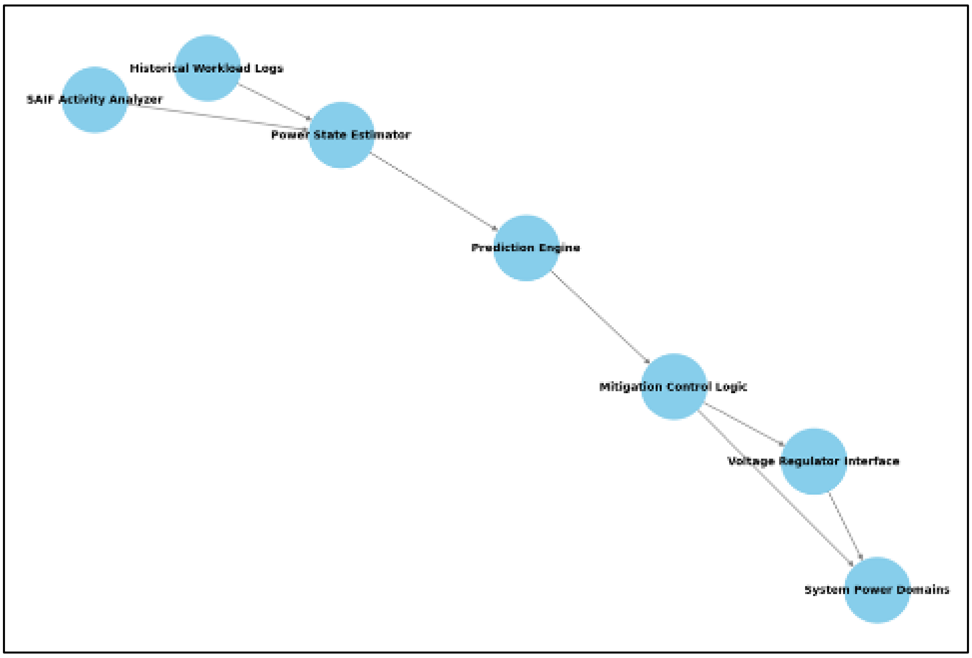
Furthermore, integrating SAIF data into power-aware verification closure enables dynamic assertions and power state-based coverage metrics to be constructed. This ensures that the design functions correctly across all critical power transitions. Such verification techniques improve first-time-right silicon success and reduce post-silicon validation costs.

4. Predictive Power Management through AI-Driven Models

Another significant advancement in SoC power management is the use of predictive models that anticipate energy requirements based on workload parameters and environmental conditions. Recent developments include transformer-based hybrid prediction algorithms, initially applied in automotive fuel cell systems but now increasingly adopted in electronic systems due to their high precision and data adaptability. These AI models integrate SAIF data to achieve fine-grained and reliable predictions [3].

These models analyze historical switching behavior to anticipate future activity rates and trigger proactive power-saving actions such as clock gating, power gating, or frequency scaling. Since SAIF reflects realistic circuit behavior rather than approximations, the predictive models achieve higher accuracy. In SoC implementations, this enables predictive strategies such as dynamic workload migration and adaptive voltage scaling before power anomalies occur.

Figure 1 illustrates the architecture of a hybrid predictive energy management system adapted for SoC environments. The model leverages historical SAIF data, voltage regulator feedback, and real-time performance metrics to adjust power states proactively.



Source: Adapted and redrawn from [3]

Figure 1 Architecture of SAIF-integrated Predictive Power Management System

This diagram demonstrates the flow of data between the SAIF analysis module, the power state estimator, and the control logic responsible for implementing mitigation actions. Such frameworks are particularly valuable in edge computing and real-time embedded systems where power budgets are tight, and responsiveness is critical.

5. Power-Aware XR Rendering and Distributed Processing

Power-aware computing is not confined to traditional computing platforms. Emerging technologies such as Extended Reality (XR) demand distributed processing under high performance requirements with limited power budgets. In this context, distributed scene rendering engines must adapt to user context, bandwidth, and the power consumption of both local and remote hardware units. SAIF-guided analysis contributes by modeling switching activities at distributed nodes and guiding load-balancing mechanisms accordingly [4].

Efficient utilization of power budgets is achieved through adaptive rendering fidelity, supported by power profiling features within scene rendering engines to ensure optimal user experience. For example, SAIF-guided analysis can detect significant IR drop within a compute cluster and shift workloads to a cooler or less congested cluster. This prevents localized overheating and extends system lifetime.

Moreover, power state modeling is incorporated as a Quality-of-Service (QoS) metric within task allocation algorithms in power-conscious scene providers. This ensures that power integrity is maintained even under high-load and high-fidelity image generation scenarios. The effectiveness of such procedures has been demonstrated in XR-related standards, which highlight improvements in both energy consumption and usability.

6. Survey of Low-Power Techniques in ASIC and FPGA Design

Extensive literature on ASIC and FPGA systems has documented various power-saving mechanisms. These include clock gating, operand isolation, multi-threshold voltage (Multi-Vt) design, and power gating. These methods can be further enhanced when guided by actual switching activity observed in SAIF files. Dynamic gating aligned with real-time SAIF traces, rather than static definitions, ensures that clock and power domains are disabled only when genuinely idle, thereby avoiding performance degradation and maximizing energy savings [5].

Table 1 below summarizes various power-saving techniques and their integration with SAIF-guided data.

Table 1 Low-Power Design Techniques and SAIF Integration

Technique	Domain	SAIF Integration Method	Benefit
Clock Gating	RTL / PnR	Signal activity thresholds	Dynamic idle detection
Operand Isolation	RTL	Activity-based control signals	Reduced unnecessary toggling
Power Gating	Physical design	Block-level switching data	Aggressive power shut-off during idle
Multi-Vt Cells	Synthesis	Switching frequency analysis	Leakage reduction in low-activity paths
DVFS	SoC level	Time-series SAIF profiling	Frequency and voltage adaptation

Source: Adapted from [5]

This classification reveals how SAIF-based activity information can enhance both architectural and physical-level design strategies. In modern SoCs, the combination of multiple techniques, each tuned by switching data, leads to significant cumulative power savings without impacting performance.

7. RTL-Level Optimizations and Multicore Power Profiling

Register Transfer Level (RTL) optimization is a fundamental component of low-power SoC design. Notable RTL-level techniques include fine-grained clock gating, conditional signal propagation, and workload-aware register activation. These techniques are particularly important in multicore RISC-V-based embedded systems and battery-powered devices. Their effectiveness is significantly enhanced when guided by SAIF data, as switching activities can be observed at signal-level granularity [6].

When SAIF traces are generated during RTL simulation, designers gain insight into which modules are heavily utilized and which remain idle under various workloads. This information enables logic synthesis tools to apply aggressive clock gating to inactive logic blocks, thereby reducing both dynamic and leakage power. In multicore environments, SAIF data can also correlate core activity with interconnect usage, providing additional opportunities to optimize power consumption within the Network-on-Chip (NoC) layer.

Furthermore, switching activity analysis supports RTL-level decisions regarding power domain partitioning. Inactive blocks can be clustered into separate power domains and power-gated accordingly. This approach is particularly beneficial in wearable and medical-grade SoCs, where power budgets are limited and battery life is critical.

Imbalanced load distribution may cause premature degradation of power delivery components in battery-based systems. SAIF-guided partitioning mitigates such risks by smoothing the power usage profile and minimizing localized current peaks. The resulting power efficiency improvements are reflected in simulation results, where enhanced energy uniformity is evaluated across the chip layout [6].

8. AI-Driven Power Estimation in FPGA Systems

Power estimation has traditionally relied on fixed spreadsheets or simulation-based models. However, the integration of artificial intelligence into design flows has significantly advanced power modeling techniques. Recent methods employ neural networks trained on SAIF-generated activity vectors to predict power consumption across different configurations in FPGA-based systems [7].

These AI-based models process RTL design parameters, SAIF activity logs, and placement information to accurately estimate power without requiring time-intensive post-layout simulations. This approach significantly reduces early design iteration time and enables rapid exploration of design alternatives.Power estimation has traditionally relied on fixed spreadsheets or simulation-based models. However, the integration of artificial intelligence into design flows has significantly advanced power modeling techniques. Recent methods employ neural networks trained on SAIF-generated activity vectors to predict power consumption across different configurations in FPGA-based systems [7].

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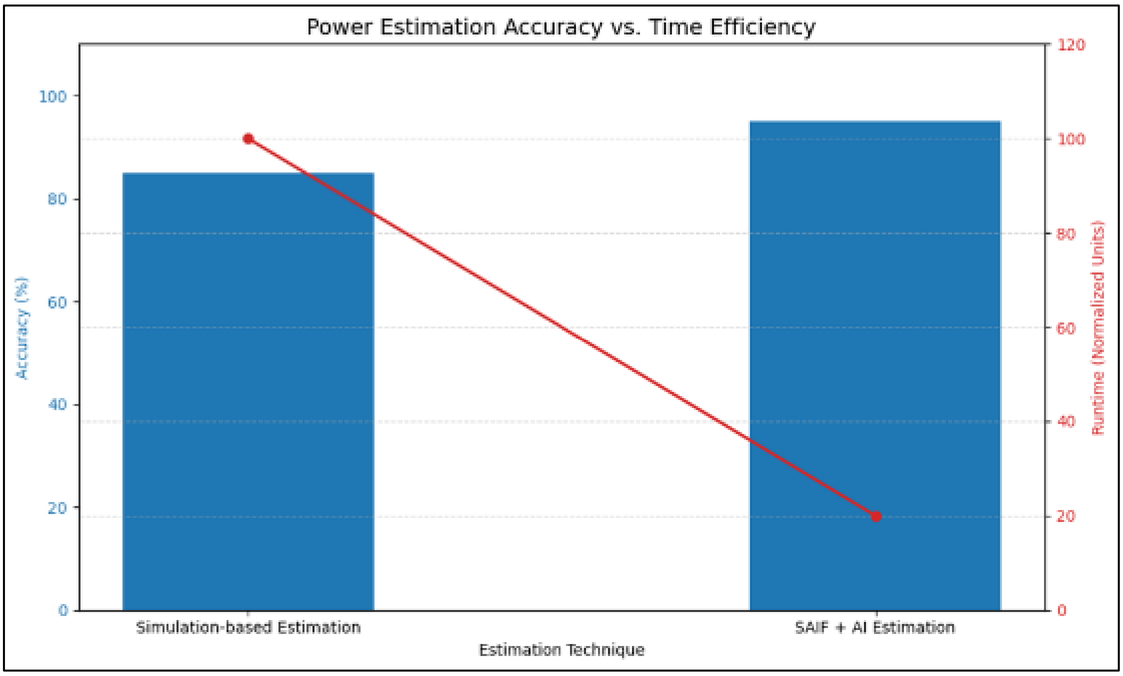

Source: Adapted and redrawn from [7]

Figure 2 Power Estimation Accuracy vs. Time Efficiency

As shown in the graph, SAIF-guided AI estimation achieves close to 95 percent accuracy compared to final sign-off tools while consuming only a fraction of the runtime. Such efficiency is pivotal for projects with aggressive schedules or resource constraints.

Besides being fast and precise, AI-based models can be power-awareness optimized through reinforcement learning where the estimator is a reward function that rewards the search of design-space. This combination between SAIF and AI can aid in bringing the power estimation further down the design curve and makes the choices taken in the earlier decision and informed.

9. Post-Design Optimization and SoC-Level Adjustments

Even after physical design completion, residual power issues may remain, particularly in high-consumption blocks such as memory controllers or high-speed serializers. Post-design optimization is therefore essential to ensure compliance with power budgets. At this stage, SAIF-guided analysis can identify abnormal switching patterns that earlier modeling stages may have overlooked [8].

Post-layout IR drop analysis often reveals hotspots that were not evident in earlier simulations due to parasitic effects and routing congestion. Designers use these insights to implement localized fixes such as cell spreading, metal layer reinforcement, or dynamic power rebalancing. The effectiveness of these corrections can be verified by comparing pre- and post-analysis layouts using SAIF-based activity data.

Additionally, SAIF data can be incorporated into Engineering Change Order (ECO) flows, enabling targeted modifications without disrupting timing closure. Minor logic or routing adjustments informed by updated switching profiles allow power improvements without full design reruns, preserving project timelines.

Post-design adjustments, such as driver strength tuning and buffer optimization based on SAIF-derived transition density reports, are commonly applied to high-speed SoC blocks. These refinements improve signal integrity while minimizing dynamic power dissipation caused by excessive capacitive loading.

10. Power Optimization in Narrowband-Broadband Hybrid SoCs

Specialized SoCs often include hybrid narrowband-broadband communication interfaces used in electric power sensing networks. Mixed-domain designs introduce additional challenges in power optimization due to variable operating modes and, in some cases, elevated activity levels. SAIF analysis facilitates the development of mode-sensitive power management systems optimized according to actual usage patterns [9].

Activity patterns in such SoCs differ significantly across sensing, transmission, and idle periods. SAIF files can be generated for each functional mode, enabling accurate determination of high-power transition paths. Designers can use this information to configure programmable power domains that shut down idle circuits. Additionally, cache behavior can be optimized to minimize dynamic power and access latency by analyzing memory access patterns derived from SAIF files.

The integration of SAIF analysis with communication stack architecture enables the implementation of power-aware link adaptation protocols and modulation schemes. For example, bursts of high activity can trigger bandwidth scaling, while low-activity periods can initiate a transition to narrowband operation to conserve power without compromising data quality.

In hybrid systems, both baseband processing units and analog front-end modules benefit from SAIF-guided optimization, allowing designers to maintain balanced energy profiles across analog and digital domains. This comprehensive power-aware integration significantly enhances the performance and efficiency of IoT-based surveillance systems.

11. SoC Validation and Functional Power Testing

SoC designs must undergo rigorous power and functional integrity testing before fabrication. Emulation platforms such as VTEST enable real-time monitoring of switching activity under functional workloads. Raw SAIF files generated during validation provide realistic and final-stage power profiling data [10].

By analyzing these SAIF traces, engineers can verify that implemented power management strategies—such as clock gating, DVFS, and domain partitioning—operate as intended under realistic execution conditions. Validation frameworks use SAIF files to compare simulated activity with emulated execution, detect discrepancies, and refine predictive models accordingly.

Emulation systems also allow testing under corner-case conditions across varying voltage and temperature ranges. During these tests, SAIF-guided IR drop analysis evaluates power delivery behavior under stress, ensuring compliance with JEDEC or AEC-Q100 standards.

This methodology has proven particularly effective in high-reliability systems such as automotive SoCs and medical devices, where power integrity is directly linked to system reliability. Integrating SAIF into the hardware verification cycle significantly reduces the likelihood of latent power-related defects reaching production.

12. Clock-Gating Mechanisms in Ultra-Low Power SoCs

Clock gating plays a critical role in reducing dynamic power consumption in ultra-low-power SoCs used in wearable and sensor applications. Hybrid clock-gating approaches combine fine-grained gating at leaf cells with coarse-grained gating at higher hierarchical levels. The strategic placement of gating logic can be effectively guided by SAIF data, which reflects actual activity patterns of functional units [11].

In practice, designers analyze SAIF reports to identify signals and modules with extended idle periods. This information is used to insert gating elements into RTL and gate-level netlists. The effectiveness of gating is validated through regression simulations that estimate dynamic power reduction using updated SAIF files.

One key advantage of SAIF-guided hybrid clock gating is adaptability. Updated SAIF files generated from newly profiled software workloads can be fed back into the gating control logic, enabling real-time reconfiguration of gating strategies. This dynamic gating capability is particularly valuable in unpredictable usage environments, such as biomedical monitors or smart wearable devices.

Hybrid clock gating can achieve dynamic power reductions of up to 40 percent without compromising performance by eliminating unnecessary clock toggling in idle logic. The importance of SAIF data in enabling this optimization is evident throughout the SoC lifecycle.

13. Conclusion

The integration of SAIF-guided in-design IR analysis within the Place-and-Route flow represents a transformative advancement in power-aware SoC implementation. By incorporating switching activity awareness from early design stages and maintaining it through verification, optimization, and validation phases, SoC designers can proactively address IR drop and power integrity challenges.

The integration of AI-driven estimation, hybrid clock gating, dynamic mapping heuristics, and mode-sensitive power control forms a holistic solution that bridges the gap between RTL and silicon. As SoC complexity continues to increase, embedding activity-driven analysis into every phase of the design process will be essential for achieving efficient, reliable, and scalable silicon solutions.

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