International Journal of Science and Research Archive
eISSN: 2582-8185
Cross Ref DOI: 10.30574/ijsra
Journal homepage: https://ijsra.net/

(REVIEW ARTICLE)

Check for updates

A hysteresis current control PWM for PV tied Z-source NPC-MLI fed induction motor with neutral point balancing

Suresh Kumar Annam [1,*] and N. Yadaiah [2]

[1] *Department of Electrical and Electronics Engineering, Samskruti College of Engineering and Technology, Hyderabad 501301, India.*
[2] *Department of Electrical and Electronics Engineering, JNTUHCEH, Hyderabad 500085, India.*

International Journal of Science and Research Archive, 2022, 07(02), 542–554

Publication history: Received on 16 November 2022; revised on 25 December 2022; accepted on 28 December 2022

Article DOI: https://doi.org/10.30574/ijsra.2022.7.2.0339

Abstract

Photo-voltaic (PV) tied Z-source Neutral-point clamped NPC-MLI (Z-NPC-MLI) is used in solar grid connected applications due to its improved performance related to conservative inverters due to its single stage power conversion. Though the Z source inverters adaptation is accepted in grid connected technology, the need for appropriate controller to meet out the grid/standalone requirements is becoming necessary. The space vector pulse width modulation (SVPWM) strategy is a prominent modulation technique for Z-source NPC-MLIs due to their appropriate voltage vector selection opportunity. The current controller (CC) based SVPWM is not attempted, which is the most essential consideration for the grid connected inverter to provide a low harmonic distortion, high quality current. With all this aim, the paper presents a PV tied Z-NPC-MLI grid connected system with a unique hysteresis current control SVPWM (HSVM) strategy with neutral point (NP) balancing control. The simulation results are confirmed the feasibility and reliability of the proposed CC for the PV tie grid connected Z- Source MLI.

Keywords: Z source MLI; Neutral-point clamped inverter; Space Vector PWM; Hysteresis current controller; Neutral Point Balancing

1. Introduction

Renewable resource (RER) is inevitable in the current power generation system (PGS) era Global solar PV capacity is expected to hit 800GW soon [1]. The photo-voltaic (PV) power generation needs a two-stage power conversion (DC to DC by buck-boost converters and DC to AC by inverters). Nevertheless, due to this two-stage power conversion and converters usages, the overall system cost and efficiency is not desirable, since it is involve more active and passive components [2]. After the arrival of Z source inverters [3], the two-stage power conversion (DC to DC and DC to AC) is made possible through single stage (DC to boosted AC), which reduced the circuit size, losses and cost. Hence Z-source inverter is considered an interesting topology for drives and PV applications [4-6] The combining Z source concept with multilevel inverters (MLIs) is most successful [7, 8]. Particularly, Neutral-point clamped (NPC) MLI is the good choice among other MLI topologies due to their circuit structure and operation is quite similar to conventional six switch voltage source inverter (VSI) [9].

In Z source inverter, the boost operation is decided by the shoot through (ST) switching state, in which the inverter input DC-link voltage is short via Z source inductors and capacitors [10]. When the pulse width modulation (PWM) is used in the Z source inverter, it is fully capable to handle ST events for handling the inverter internal issues such as DC-link control and THD becomes mandatory. The PWM approaches are investigated by adjusting the carrier positions and altering the shoot through (ST) for minimum, constant and maximum boosting methods [10]. The space vector pulse

* Corresponding author: Suresh Kumar Annam, Department of EEE, Samkruti College of Engineering and Technology,Ghatkesar, Telangana,India.

width modulation (SVPWM) strategy provides opportunity to deal the switching sequence directly, which facility is not in carrier based PWM. The P. C. Loh *et.al* has proposed SVPWM for controlling three-phase three-level Z-MLI with 24 ST options [11]-[20]. Followed by [12]F. B. Effah *et.al* developed a new set of ST options, where the authors used 12 ST states. These attempts have well concluded about controlling the inverter voltage. However, the current control is not attempted which the main factor of dc-link capacitor is balancing [23].

The PV tied grid system requires a stable power converter, current controller and PWM technique for the straight forward operation, less cost, and high performance. In context with capacitor balancing in Z source NPC, few examples found in [26-28] using SVM and carrier level-shifted based control, which are not discussed current control.

With this motivation, this paper suggests the three-phase three-level PV connected transformerless Z source-MLI for the utility grid. The Hysteresis SVPWM (HSVM) is designed for the grid synchronization. The proposed HSVM avoids the switching shoot through and eliminates the low frequency oscillations using suitable ST (Upper and Lower ST), with regular switching events, which ensures the DC-link capacitors balancing along with current control. The proposed system is simulated and verified through MATLAB/Simulink software. The laboratory prototype 2-kWp solar panels attached grid connected three-phase three-level Z-NPC-MLI is established and the validation is done through Xilinx family SPARTAN-6 controller. The results obtained from the simulation and experiment is confirming the technical feasibility and advantages of the proposed HCC. In addition the results have shown the uniqueness of the proposed current controller involvement with SVPWM for improving the inverter performance.

2. Z-source NPC-MLI power circuit

This session explains the Z-NPC-MLI power circuit and its operation.

2.1. Z-NPC-MLI

The Fig.1 shows the power circuit of Z-NPC-MLI in three-phase three-level structure, which consists of three legs, and each leg has four power switches (S_{1A}– S_{4A}) with 2 clamping diodes (D_{A1} and D_{A2}). The Z source impedance elements (L_1=L_2=L, C_3 =C_4=C) are connected in the input side and obtaining power from DC-link. Two DC-link capacitors (C_1&C_2) are serially coupled with DC input source, which split the DC-link voltage as $V_{DC}/2$ for making the multilevel output as 0, $V_{DC}/2$, and V_{DC}. In the load side, each inverter leg is connected to grid by using inductor (L_A=L_B=L_C=L_g). The Z-NPC-MLI is operating with shoot through (ST) and non-shoot through (NST) mode. In ST mode, the input DC supply is shorting through inverter switch and X –network inductors, to store the energy in the inductors, L_1 and L_2. During NST mode, the DC power is converted to AC power (through normal inverter switching).

By considering one leg in NPC-MLI, the operation is described by three switch options; 1(both upper switch ON), 0(middle switch ON),-1(both lower switch ON). Including Z source operation with NPC-MLI regular switching operations, the ST mode is created in order to short the input DC supply through inductors by switching ON all the four switches in the leg, which is called as full shoot through (FST). Alternatively, for reducing the switching losses, the top ST (top 3 switches is ON in a leg) and bottom ST (bottom 3 switches is ON in a leg). The table-1 describes all the possible combinations of the switching options for Z-NPC-MLI.

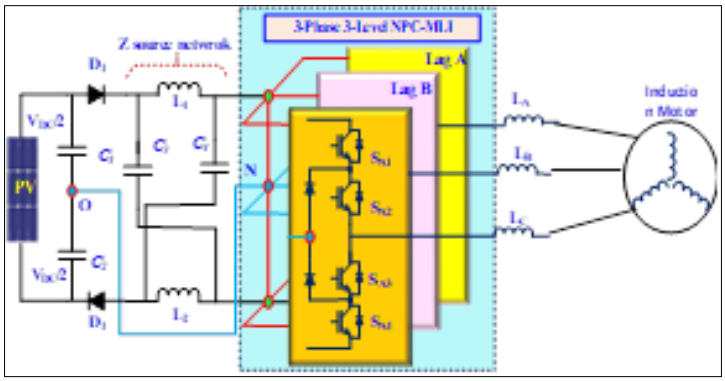


Figure 1 PV tied grid connected three-phase three-level Z source NPC-MLI fed IM

2.2. ST and NST operation of Z-NPC-MLI

The ST and NST mode operation power circuitry is shown in Fig.2. During the ST mode, the inverter can be involved either full ST or partial ST [26]. Though this both the methods are shorting the input DC source via inductors L_1 and L_2, the full ST(FST) is not a best choice of balancing the inductors charging profile (nonlinearity charging) and it roots high lower order harmonics in the output waveforms. Since the Upper-ST(UST) and Lower-ST(LST) has an individual control on the L_1 and L_2 charging characteristics, the combination of UST and LST maintains the inductors charging in parallel, which ensures the better-quality output waveform [7,11].

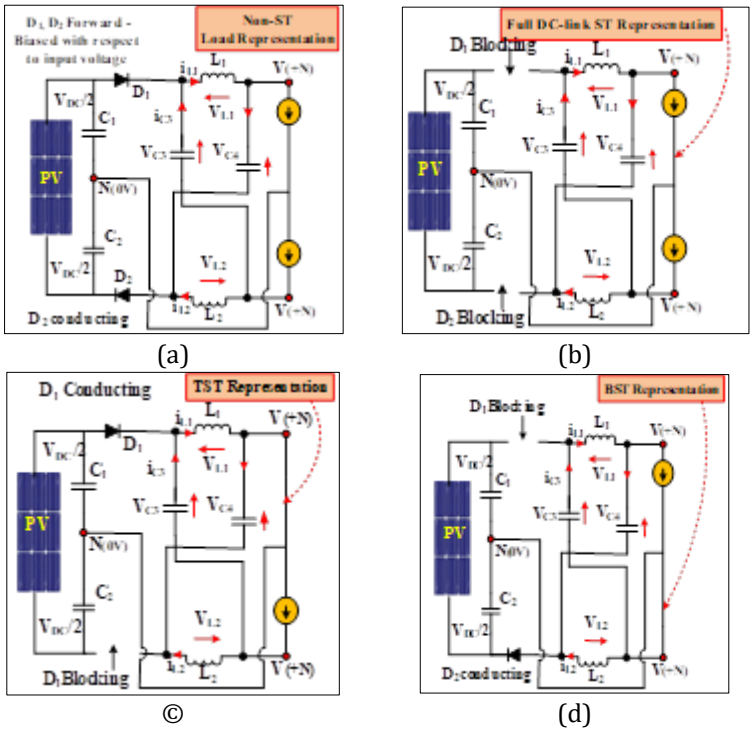


Figure 2 ST and NST mode operation of Z source NPC-MLI; (a) Non-ST (NST),(b) full-ST,(c)UST,(d)LST

2.3. Design Analysis of Z source network

For any Z network, calculation of their X network elements (L and C) and its charging, discharging and boosting functions are important. During ST period, while considering the symmetry charging and discharging nature on L (L_1=L_2=L) and C (C_3=C_4=C), the voltage across the inductors and capacitors are approaches to V_L and V_C respectively, where V_{L1} =V_{L2}=V_L=

Table 1 ST and not ST operation of Z-NPC-MLI

Mode	Switching State	Tuned on switches	Action	Vout
NST	+1	SX1 SX2	-	(VDC/2)+L1*(di/dt)
	0	SX2 SX3	-	0
	-1	SX3 SX4	-	-(VDC/2)-L2*(di/dt)
ST	Full ST	SX1 SX2 SX3 SX4	Charging L1 & L2	0
STT	Top ST	SX1 SX2 SX3	L1 Charging	0
STB	Bottom ST	SX2 SX3 SX4	L2 Charging	0

$L_1(di/dt) = L_2(di/dt)$ and V_C=V_{C3}=V_{C4}= $V_{DC}/2$.

During the NST mode, $V_L = V_C = V_{DC}/2$. This condition is satisfied, since the capacitors C_1 and C_2 are connected in parallel and voltage across the Z source network will be $2V_C$. In ideal conditions, $V_L = V_C$ and $2V_C = 2V_{dc}$. During this condition, the inverter output voltage, $V_o = 0$.

From the Fig 2, considering ST mode of operation (see Fig.2.a); when diode D_1 and D_2 are in forward bias conduction,

The inductor voltage,

$$V_{L1} = V_{DC} - V_C \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$V(+) \Longrightarrow \frac{V_i}{2};\ V(-) \Longrightarrow -\frac{V_i}{2} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$$V_i = 2V_C - V_{DC} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

During UST mode operation as shown in Fig.2.c, the diode $D_1$is in conduction and D_2 is in blocking state. Hence the inductor voltages are obtained as,

$$V_{L1} = \frac{V_{DC}}{2}; V_{L2} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

$$\text{and, } V(+) = 0V; V(-) = \frac{V_{DC}}{2} - V_{C3} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

During LST mode operation as shown in Fig.2.d, the diode D_2 is in conduction and D_1 is in blocking state. Hence the inductor voltages are obtained as,

$$V_{L1} = 0; V_{L2} = \frac{V_{DC}}{2} \quad \ldots\ldots\ldots\ldots\ldots\ldots (6)$$

$$\text{and, } V(-) = 0V; V(+) = -\frac{V_{DC}}{2} + V_{C4} \quad (7)$$

During UST and LST, the voltage present in the DC-link is half that of NST. Hence, it is proven that by equally sharing UST and LST mode using input DC-link capacitors (C_1 and C_2), the inverter is boosting voltage with proper DC-link balancing, which helps the THD performance on the output voltage and current waveform.

The inverter pack ac voltage output, Vx_0 (x={A<B<C}) is resulting as,

$$V_{x0} = \frac{M}{\sqrt{3}} V_{i\_NST} \quad \ldots\ldots\ldots\ldots\ldots\ldots (13)$$

$$V_{xo} = \{\frac{M}{\sqrt{3}} V_{DC}\} \frac{1}{\left(1 - \frac{T_{TST} + T_{BST}}{T}\right)} = \{\frac{M}{\sqrt{3}} V_{DC}\} B_F \quad \ldots\ldots\ldots\ldots\ldots\ldots (14)$$

Where B_F is boosting factor ($B_F \geq 1$).

3. Proposed SVPWM FOR Z-NPC-MLI

This session explains the proposed current SVPWM including the capacitor balancing Z-NPC-MLI and its operation.

3.1. Operation of SVPWM

The Fig. 3 shows the three-level space vector diagram (SVD) with their different switching state vectors. For normal inverter operation (during the NST mode), the inverter has four different switching vectors (zero vector {ZV}, small vector {SV}, medium vector {MV}, and large vector {LV}) to bring multilevel output voltage [22]. These four switching vectors are forming hexagon (called space vector diagram) using their 27 switching states, among which one for ZV, 12 for SV,6 for MV and 6 for LV.

According to the SVD presented in Fig. 7, in every switching action have an individual phase current, which affects the DC-link capacitors/NP balancing. For example, at SV switching state [100], the B and C phases are linked with neutral point 'O' and phase-A is associated to input DC link. Hence, neutral current ($I_N = i_A + i_B + i_C$) is approach to $-i_A$ ($i_B + i_C = -i_A$).

For balanced DC-link condition, the I_N should be zero. Table-II shows the different switching's phase current for the three-level NPC-MLI. Here, the ZV and SV have redundant switching privileges, which help balancing the DC-link. However, the MV and LV has only unique switching option for a sector. Hence these vectors not helping for NP self-balancing. The Fig.4 shows the SVD with their different switching states of ZV, SV, MV and LV including phase currents

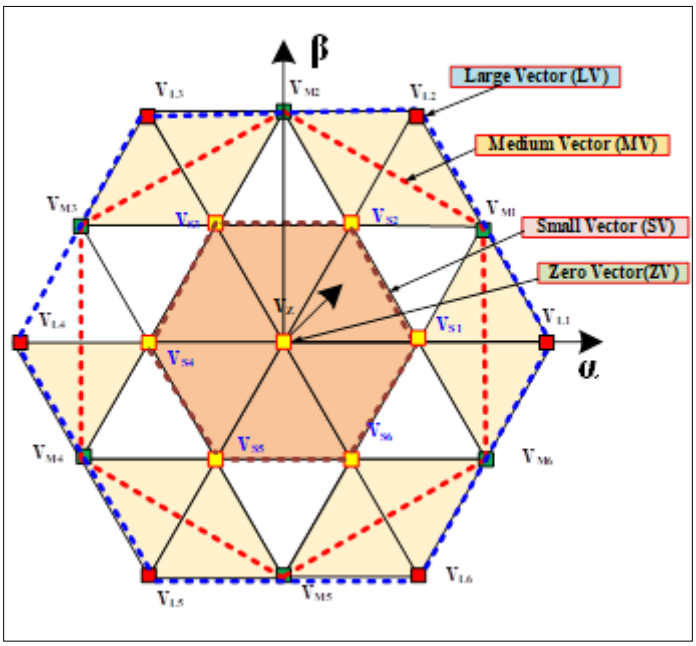
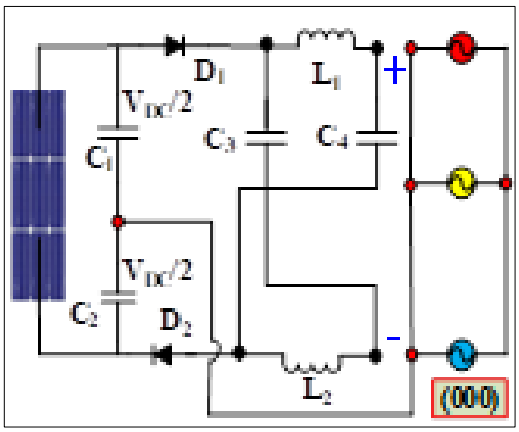
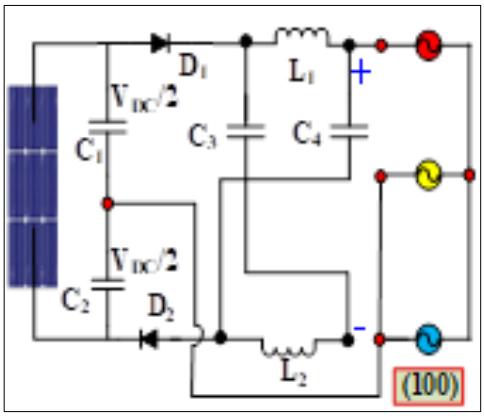


Figure 3 SVD of three-phase three-level Z-NPC-MLI

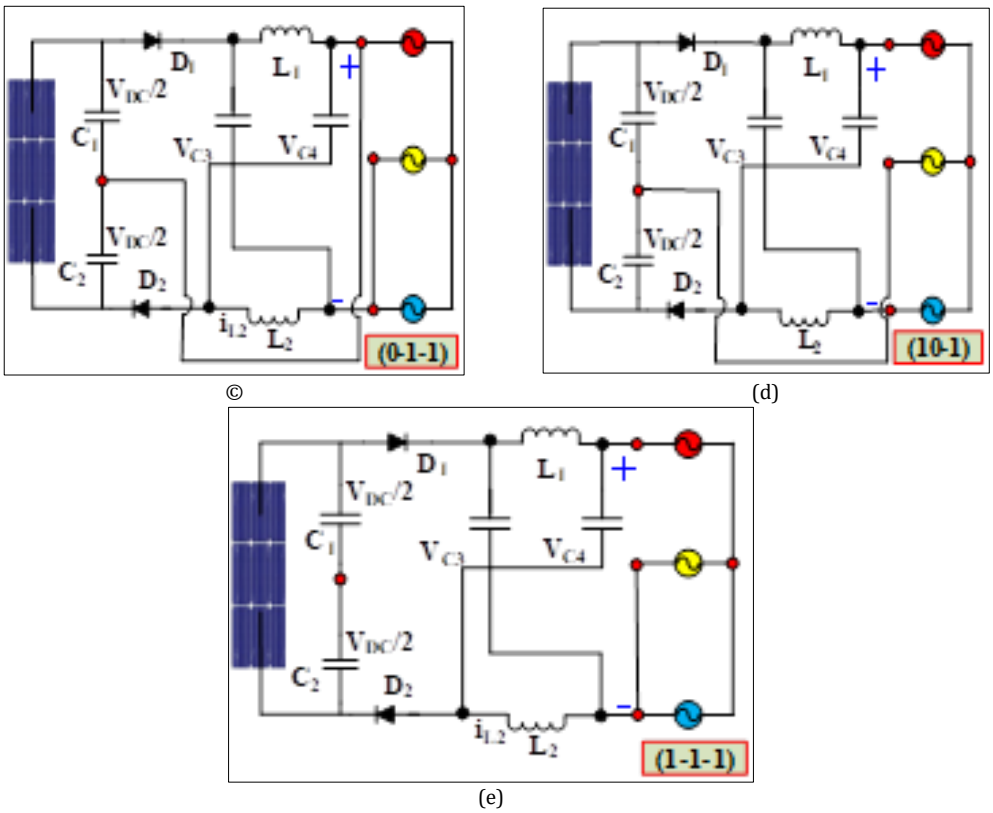
According to the SVD presented in Fig. 7, in every switching action an individual phase current is producing, which affects the capacitors/DC-link balancing. For example, at SV switching state [100], the B and C phases are linked with neutral point 'O' and phase-A is associated to input DC link. Hence, neutral current ($I_N=i_A+i_B+i_C$) is approach to $-i_A$ ($i_B+i_C=-i_A$). For balanced DC-link condition the I_N have to be zero. Table-II shows the different switching phase current for the SVD. The ZV and SV have redundant switching prestige, which help balancing the DC-link. The Fig.4 shows the SVD with their different switching states of ZV, SV, MV and LV including phase currents. Now, for creating UST and LST, the proposed SVPWM is considering SVs since they have a redundant switching prestige which helps the inverter DC-link balancing.



(a)



(b)



© (d) (e)

Figure 4 NST switching state of Z source NPC-MLI;(a) ZV[000] ,(b) positive current SV[100] ,(c) positive current SV[0-1-1],)(d) MV[10-1],(e)LV[1-1-1]

Table 2 ST and not ST operation of Z-NPC-MLI

(+)ve SVs	i_{NP}	(-) ve SVs	i_{NP}	MVs	i_{NP}	LVs	i_{NP}	ZVs	i_{NP}
[0-1-1]	i_A	[1 0 0]	$-i_A$	[1 0-1]	i_A	[1-1-1]	0	[111]	0
[-10-1]	i_B	[0 1 0]	$-i_B$	[0 1-1]	i_B	[11-1]	0	[000]	0
[0 0-1]	i_C	[1 1 0]	$-i_C$	[-1 10]	i_C	[-11-1]	0	[-1-11]	0
[0 1 1]	i_A	[-10 0]	$-i_A$	[-1 01]	i_A	[-111]	0	-	-
[1 0 1]	i_B	[0-1 0]	$-i_B$	[0-1 1]	i_B	[-1-11]	0	-	-
[-1-10]	i_C	[0 0 1]	$-i_C$	[1-1 0]	i_C	[1-11]	0	-	-

3.2. Operation of source Z-NPC-MLI SVPWM

The Fig.5 shows the ST creating switching prominence. The UST and LST chosen based on switching state transition. Considering sector-1 sub-triangle $\Delta_{1,4}$ as shown in Fig.5, the regular MLI switching paten is {[0-1-1], [1-1-1], [10-1], [100], [10-1], [1-1-1], [0-1-1]}. Here, considering proposed Z-MLI, ST is fixed through changes in the adjacent switching state. For example, the 1st switching state [0-1-1] and their next [1-1-1] the transition is only on A-phase switching (0→1). Therefore, the ST is fixed through UST in A-phase and fixed between [0-1-1] and [1-1-1]. Similarly, in the same Δ_{14} switching states series the [10-1] and [100] differs from their C-phase. Hence the next ST is fixed through LST in C-phase and fixing in between [10-1] and [100]. The UST and LST selections are chosen based on the current flow directions on the inverter from DC-link to load. When, bit change in 0→1, the UST is chosen and when the bit change in -1→0, the LST has chosen. The ST interval for both UST and LST is depend on the boosting factor using Eq(12). Here in order to maintain the NP self-balancing and volt-sec balancing, the inverter switching selections are starting from A-phase to C- phase in a forward switching and following the reverse same sequence order. The UST and LST switching

states timing is sharing from the regular switching, which ensure the symmetry output voltage. For example, when the target vector lies in $\Delta_{1,4}$, the UST is time calculated from the boosting factor and fixed between [0-1-1] and [1-1-1] without changing switching frequency. Using this method, the number of power switching commutations in a switching cycle is same as traditional NPC-MLI, which ensures the switching losses in the Z-NPC-MLI. In this method, when the inverter is operating in lower modulation index (M_a)/ buck mode, there is no STs are inserted. Therefore, this is ensuring the avoidance of line to line collapse in inverter line to line voltage and NP. Next section discusses the proposed HCC.

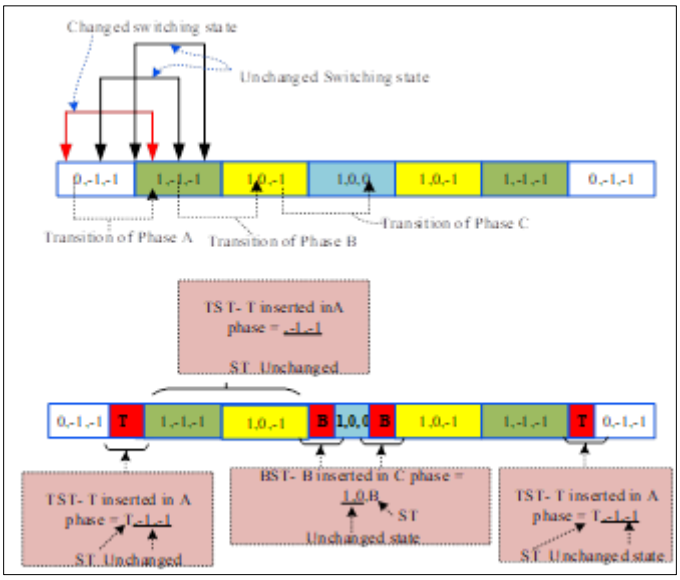


Figure 5 $\Delta_{1,4}$ ST switching state creation for Z-NPC-MLI

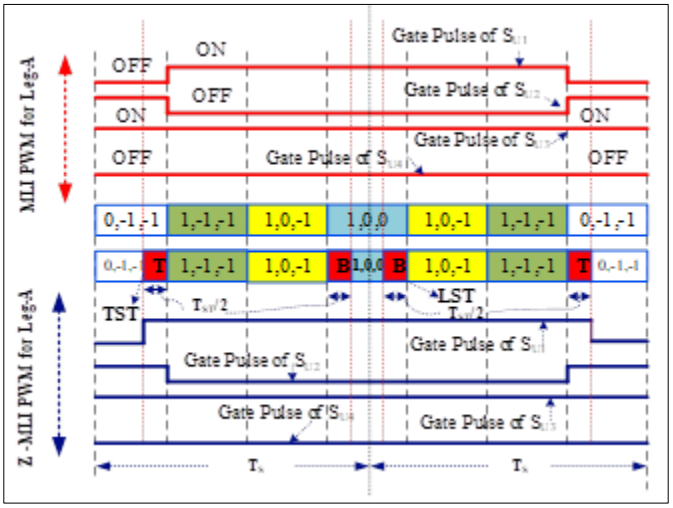


Figure 6 $\Delta_{1,4}$ ST and NST switching state and PWM pulse for Z-NPC-MLI

3.3. HSVM

In proposed SVPWM current control method, the hysteresis bands are directly used to employ the four groups of (ZV, SV, MV and LV) vectors in SVD. Here the current controls made based on current error (error vector$\overrightarrow{\Delta_i}$) and available switching options on SVD. The proposed structure is principally employed to retain the $\vec{i}_{Lact}$ close to the $\vec{i}_{Lref}$ inside circular hysteresis band values. To compensate for the complication of achieving the CC along with capacitors balancing, the SVPWM is modified based on the hysteresis band 'H'.

Fixed frequency HCC can be obtained by calculating the hysteresis band H using the transient value of the V_g and output voltage of PV array.

Based on that, the hysteresis band 'H' is calculated as,

$$H = \frac{V_g(V_{PV} - 2.V_g)}{V_{PV}.L.f_s} \text{.....(15)}$$

Here the variant parameters are V_{PV}, V_g, f_S and fixed one is filter inductor (L). Here, when the reference current (i_{Lref}) and actual current (i_{Lact}) lie in SVD error vector, $\vec{\varepsilon_i}$ is calculated as,

$$\vec{\varepsilon_i} = \overrightarrow{i_{Lref}} - j\,\overrightarrow{i_{Lact}} \text{..... (16)}$$

Where, $\overrightarrow{i_{Lref}} = i_{Lref\,\alpha} + j\, i_{Lref\,\beta}$; $\overrightarrow{i_{Lact}} = i_{Lact\,\alpha} + j\, i_{Lact\,\beta}$

When the $\vec{\varepsilon_i}$ expressed in the SVD plane with αβ-vector components frame, the $\vec{\varepsilon_i}$ can be represented as,

$$\vec{\varepsilon_i} = \overrightarrow{\Delta_{i\alpha}} + j\,\overrightarrow{\Delta_{i\beta}} \text{..... (17)}$$

From Eq (5), the position of the $\vec{\varepsilon_i}$ in SVD is calculated and then the switching vectors are selected to keep the $\vec{i}_{Lact}$ close to the $\vec{i}_{Lref}$ .Fig.8 show the HSVM with $\vec{\varepsilon_i}$ and H. Here, the sector and sub-triangle, and its switching state selection is done based on the $\vec{\varepsilon_i}$ and H. The area boundary is determined by the hysteresis bands (H_1 and H_2).

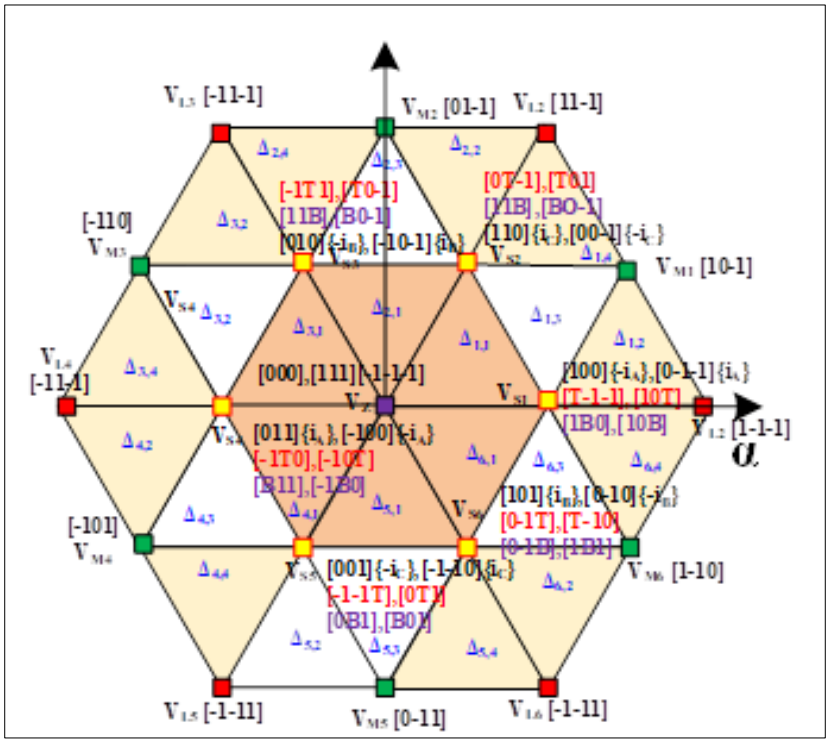


Figure 7 SVD for three phase Three Level Z source NPC-MLI including UST, LST and individual phase currents for NST switching states

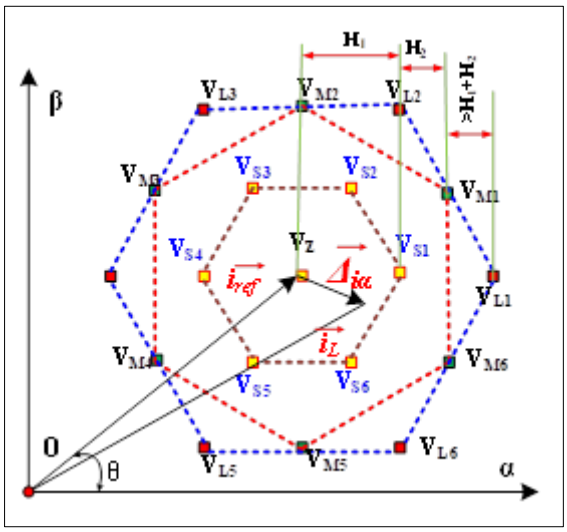


Figure 8 SVHCC for three-phase three-level Z source NPC-MLI

The values of H1 and H2 depend on $\vec{i}_{Lref}$ and its control dynamics. The values of H will vary between zero to H (Eq.15). Here the Maximum value of the H is related with maximum operation modulation (Modulation Index, M_a). To finding of the $\vec{\varepsilon_i}$ and H, the proposed SVD operating in three environments which are H_1, H_2, $>H_1+H_2$.

During the H_1 interval the switching selection is directed to use for ZV and SV. Similarly, for H_2 the SV and MV, and when H is beyond H_1+H_2, the SV, MV, LV switching states is selected.

3.4. Neutral point/dc-link balancing

In the proposed HSVM using nearest three vectors N3Vswitching selection vector selection [18,20]. Based on the $\vec{\varepsilon_i}$tip is the HSVM chose the sector and sub-triangle, and switch the vertices of the triangle in every switching period for the hysteresis region using all available vector to get zero phase current.

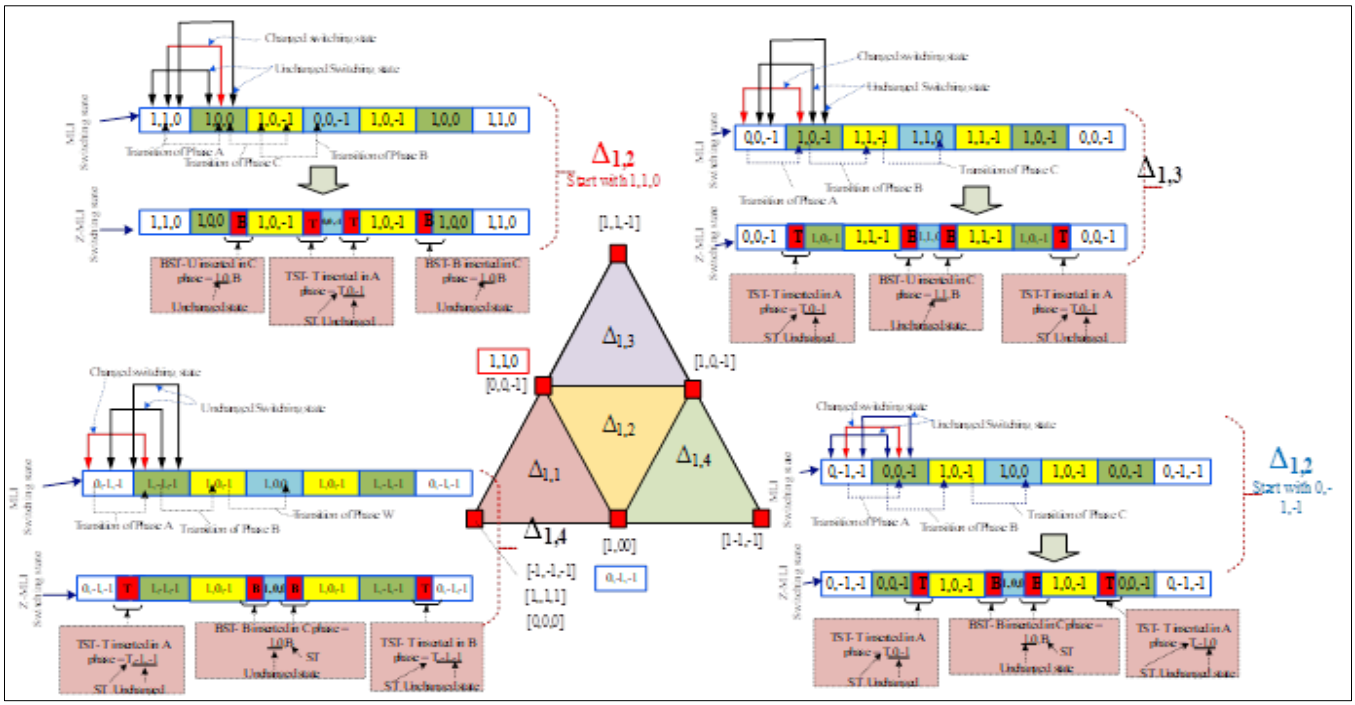


Figure 9 Sector-1 ST and NST switching state for Z-NPC-MLI

For example, if $\overrightarrow{\varepsilon_t}$ tip is situated in H_1 region, the control lies in the triangle $\Delta_{1,1}$, switching vectors, V_{Z0} {[000], [111], [-1-1-1]}, V_{S2} {[110], [00-1]} and V_{S3} {[010[, [-10-1]} are selected with their ST options. Similarly, when vector lies in $\Delta_{1,2}$, in order or to balance the NP the vector switching are chosen in redundant manner as shown in Fig.9. Here, the SV switching sequences [0-1-1], [110] has chosen as a stating switching state to synthesis the reference vector. Hence, at target reference vector lies in $\Delta_{1,2}$ the vector synthetization is happen in two time to balance the capacitor. Other sub-triangles $\Delta_{1,3}$ and$\Delta_{1,4}$ are ha only one, since they involve MV and LV. As shown in Table-1, the LV phase current is zero. However, the MV showing the particular phase current which is causes the small disturbance in DC link balancing. As per the NP fluctuation standard this is considerably small.

3.5. Simulation Study

This session explains the proposed current SVPWM with MATLAB simulation and FPGA based experimentation for 2kW laboratory setup PV fed connected Z source NPC-MLI.

3.6. Simulation Study

The performance of the proposed HSVC based PV connected three-phase three-level Z-NPC-MLI simulation models are performed using MATLAB/Simulink 11.b. Here, the 2kW PV array modules configured (series model) to feed the power to inverter with each module rated at 152.5W. The NPC-MLI maintains the dc-link voltage close to 250V by the help of two (C_1 and C_2) 470µF capacitors. The inverter is connected to 300V/50 Hz utility grid via 4 mH inductors.

The inverter switching frequency (f_{sw}) is maintained throughout the operation of the inverter as 5 kHz. Initially the Z-NPC-MLI is simulated and investigated with grid connected system with fixed hysteresis bands. At inverter boosting factor set a 1.5, the inverter approach to 331V. The Fig.10 shows the inverter line voltages and load phase current for different operating conditions (different modulation indies). During every operation instants the inverter delivers the voltage and current with minimal voltage and current THD. The Fig. 11 show the voltage and current harmonics spectra for the maximum inverter operating point, m_a=0.9. From the THD spectrum results, its confirm that the inverter maintain the minimal voltage THD (6.48%) and current THD (1.07%) , since the DC-link voltage is controlled. The Fig. 12 show actual load current and reference current tracking performance with fixed H band (5Amps). The tracking performance is executed with 50Hz and 60 Hz reference current. From the waveform, it could see that the actual current is clearly tracking the reference current with decent steady state and transient response. To validate the DC-link capacitors (V_{C1} and V_{C2}) balancing for HSVM, the simulation is performed for both conventional and proposed HSVM, which are shown in Fig.13 (a) and Fig.13. (b) Respectively. The NP fluctuation (NPF) is calculated from V_{C1} and V_{C2};

$$\text{NPF} = \frac{(\frac{V_{DC}}{2}) - V_{C1}}{(\frac{V_{DC}}{2})} \quad \ldots\ldots\ldots\ldots\ldots\ldots (16)$$

From the Eq.(16), the proposed HSVM NPF is very less (calculated as ≈1%) the conventional Z-source SVM (calculated as ≈10%), which ensure the output voltage and current waveform quality. Based on the results the proposed HSVM is claims it is not only controlling current and it is also maintaining the NP current.

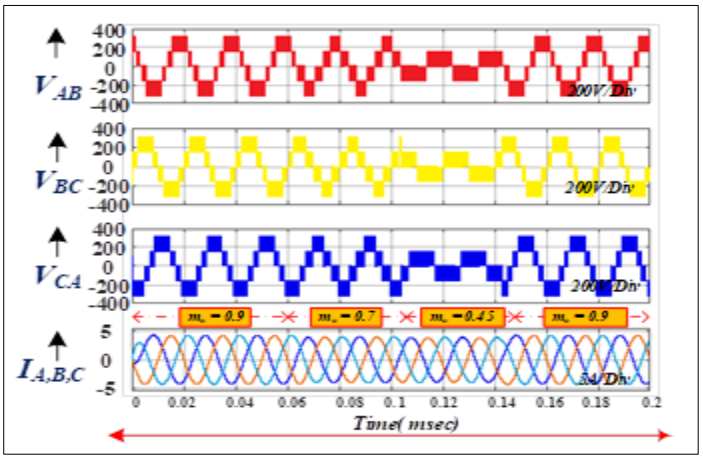
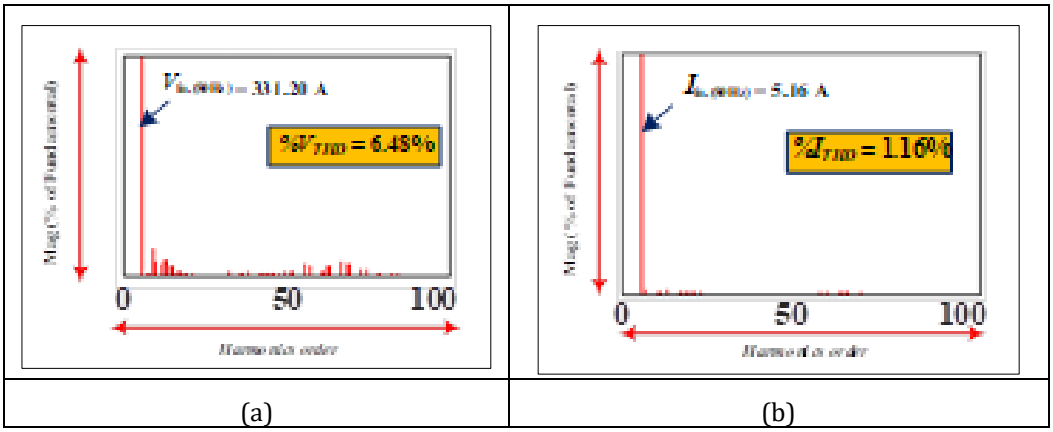


Figure 10 Simulation results of three phase voltage and current waveform of Z-NPC-MLI



(a) (b)

Figure 11 Simulation results of harmonics spectra for Z-NPC-MLI at m_a=0.9; (a) voltage harmonics spectra and current harmonics spectra

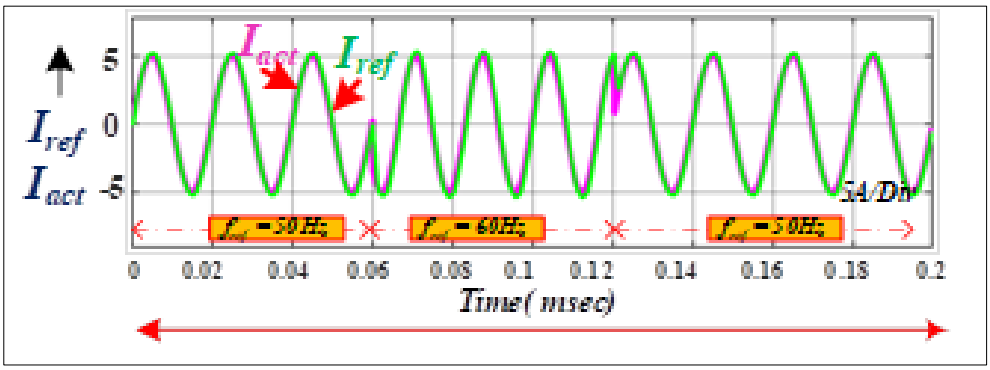
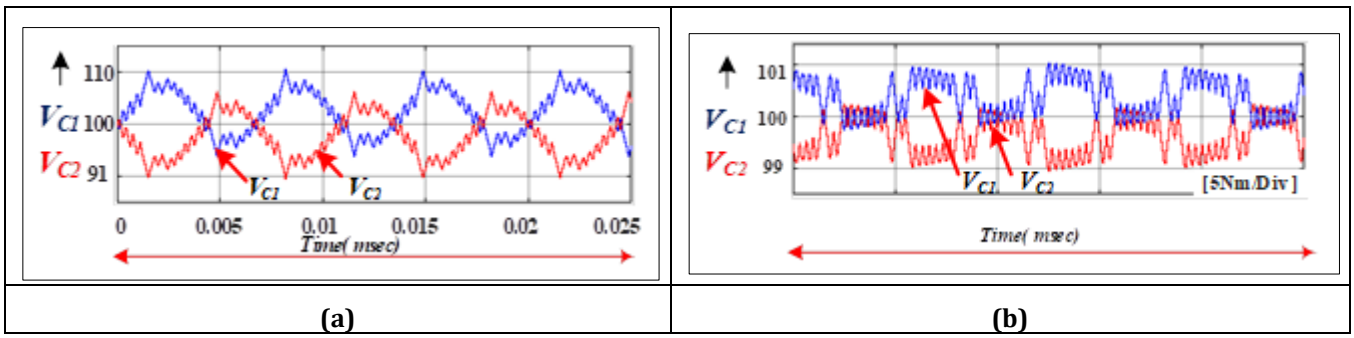


Figure 12 Simulation results of actual load current and reference current when H band is fixed at 5Amps



(a) **(b)**

Figure 13 Simulation results of Z-NPC-MLI voltage across DC-link capacitors; (a) conventional SVM method, (b) HsvM

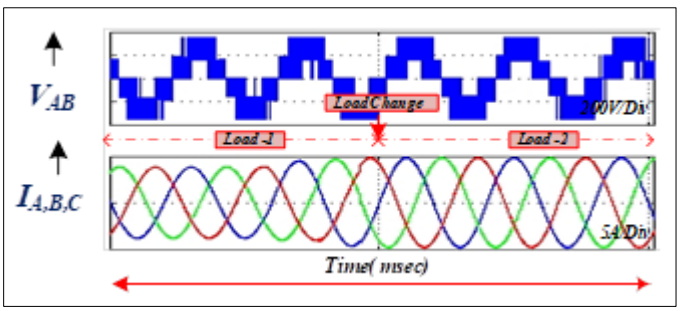


Figure 14 Simulation results -Transient response of the HSVM to change in load current magnitude

The study is further prolonged for varying hysteresis band and change in reference current frequency. Fig.14 shows the transient response of the proposed HSVM. Here, when there in the change in load current magnitude, the HSVM is gear up the boosting factor and meeting out the load voltage and current requirement together with NP balancing.

4. Conclusion

The three-level Z source NPC-MLI is analyzed for PV tie grid connected system. Through the Z-NPC-MLI and its SVPWM available in the literature, considering the adaptation in grid connected technology, the current controller handling behavior is mandatory for SVPWM. Hence, the proposed SVPWM is marge Z source SVPWM technique with hysteresis current control and offer to the grid connected PV tied Z-NPC-MLI system. Unlike previous SVPWM attempted Z-NPC-MLI, the proposed SVPWM modified the inverter ST positions and handled NP balancing effectively. The simulation and results are confirmed superiority of the proposed HSVM period.

Compliance with ethical standards

Acknowledgments

Department of EEE, JNTUH CEH, Hyderabad and Department of EEE, Samskruti college of Engineering and Technology. Ghatkesar.

Disclosure of conflict of interest

This Research work and paper is carried out jointly by the Suresh Kumar Annam and N. Yadaiah authors.

The manuscript does not have any conflict of interest exists in the submission of this manuscript, and the manuscript is approved by all authors for publication. I would like to declare on behalf of my co-author that the review paper has written and described from various original research work and papers, and is not published elsewhere, in whole or in part. We sincerely hope for your full consideration of our manuscript

References

[1] Z. Dobrotkova, K. Surana, and P. Audinet, The price of solar energy: Comparing competitive auctions for utility-scale solar PV in developing countries, Energy Policy, vol. 118, pp. 133–148, Jul. 2018.

[2] R. Teichmann and S. Bernet, A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications, IEEE Trans. Ind. Appl., vol. 41, no. 3, pp. 855–865, May/Jun. 2005.

[3] F. Z. Peng, Z-source inverter, IEEE Trans. Ind. Appl., vol. 39,pp. 504–510, Mar./Apr. 2003

[4] P. C. Loh and F. Blaabjerg, Magnetically Coupled Impedance-Source Inverters, IEEE Trans. Ind. Appl., vol. 49, no. 5, pp. 2177–2187, Sep. 2013.

[5] F. Gao, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, Dual Z-Source Inverter With Three-Level Reduced Common-Mode Switching, IEEE Trans. Ind. Appl., vol. 43, no. 6, pp. 1597–1608, 2007.

[6] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, Impedance-source networks for electric power conversion Part I: A topological review, IEEE Trans. Power Electron., vol. 30, no. 2, pp. 699–716, Feb. 2015.

[7] Yu, Q. Cheng, J. Gao, F. Tan, and Y. Zhang, Three-level neutral-point-clamped quasi-Z-source inverter with reduced Z-source capacitor voltage, Electronics Letters, vol. 53, no. 3, pp. 185–187, Feb. 2017.

[8] Poh Chiang Loh, Feng Gao, and F. Blaabjerg, Embedded EZ-Source Inverters, IEEE Trans. Ind. Appl., vol. 46, no. 1, pp. 256–267, 2010.

[9] F. Gao, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, Performance Evaluation of Three-Level Z-Source Inverters Under Semiconductor-Failure Conditions, , IEEE Trans. Ind. Appl., vol. 45, no. 3, pp. 971–981, 2009

[10] P. C. Loh, S. W. Lim, F. Gao, and F. Blaabjerg, Three-level Z-source inverters using a single LC impedance network, IEEE Trans. Power Electron., vol. 22, no. 2, pp. 706–711, Mar. 2007.

[11] P. C. Loh, F. Gao, F. Blaabjerg, S. Y. C. Feng, and K. N. J. Soon,Pulse width-modulated Z-source neutral-point-clamped inverter, IEEE Trans. Ind. Appl., vol. 43, no. 5, pp. 1295–1308, Sep./Oct. 2007.

[12] F. B. Effah, P. Wheeler, J. Clare, and A. Watson, Space-Vector-Modulated Three-Level Inverters With a Single Z-Source Network, IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2806–2815, Jun. 2013.

[13] S. V. Araujo, P. Zacharias, and R. Mallwitz, Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems, IEEE Trans. Ind. Electron.,vol. 57, no. 9, pp. 3118-3128, Sep. 2010.

[14] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression, IEEE Trans. Ind. Electron.,vol. 62, no. 7, pp. 4537-4551, Jul. 2015.

[15] T. Kerekes, R. Teodorescu, M. Liserre, C. Klumpner, and M. Sumner, Evaluation of Three-Phase Transformerless Photovoltaic Inverter Topologies, IEEE Trans. Power Electron., vol. 24, no. 9, pp. 2202-2211, Sep. 2009.

[16] P. Chaparala, Erhong Li, and S. Bhola, Reliability qualification of photovoltaic smart panel electronics, 2010 17th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, Jul. 2010.

[17] M. P. Kazmierkowski and L. Malesani, Current control techniques for three-phase voltage-source PWM converters: a survey, IEEE Trans. Ind. Electron.,vol. 45, no. 5, pp. 691-703, 1998

[18] M. A. Rahman, T. S. Radwan, A. M. Osheiba, and A. E. Lashine, Analysis of current controllers for voltage-source inverter, IEEE Trans. Ind. Electron.,vol. 44, no. 4, pp. 477-485, 1997.

[19] A. Shukla, A. Ghosh, and A. Joshi, Hysteresis Modulation of Multilevel Inverters, IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1396-1409, May 2011.

[20] C.Bharatiraja, S. Jeevananthan, S, R.Latha, and V.Mohan, Vector selection approach-based hexagonal hysteresis space vector current controller for a three phase diode clamped MLI with capacitor voltage balancing , IET Power Electron., vol. 9, no. 7, pp. 1350-1361, June 2016.

[21] T. Ghennam, E. M. Berkouk, and B. Francois, A Novel Space-Vector Current Control Based on Circular Hysteresis Areas of a Three-Phase Neutral-Point-Clamped Inverter, IEEE Trans. Ind. Electron.,vol. 57, no. 8, pp. 2669-2678, Aug. 2010.

[22] C. Bharatiraja, S. Jeevananthan, and R. Latha, FPGA based practical implementation of NPC-MLI with SVPWM for an autonomous operation PV system with capacitor balancing, International Journal of Electrical Power & Energy Systems, vol. 61, pp. 489-509, Oct. 2014.

[23] Chenchen Wang and Yongdong Li, Analysis and Calculation of Zero-Sequence Voltage Considering Neutral-Point Potential Balancing in Three-Level NPC Converters, IEEE Trans. Ind. Electron.,vol. 57, no. 7, pp. 2262-2271, Jul. 2010.

[24] Huibin Zhang, S. Jon Finney, A. Massoud, and B. W. Williams, An SVM Algorithm to Balance the Capacitor Voltages of the Three-Level NPC Active Power Filter, IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2694-2702, Nov. 2008.

[25] J.-S. Lee and K.-B. Lee, New Modulation Techniques for a Leakage Current Reduction and a Neutral-Point Voltage Balance in Transformerless Photovoltaic Systems Using a Three-Level Inverter, IEEE Trans. Power Electron., vol. 29, no. 4, pp. 1720-1732, Apr. 2014.

[26] X. Xing, C. Zhang, A. Chen, J. He, W. Wang, and C. Du, Space-Vector-Modulated Method for Boosting and Neutral Voltage Balancing in Z-Source Three-Level T-Type Inverter, IEEE Trans. Ind. Appl., pp. vol. 52, no.2, pp. 1621 - 1631, March/April 2016.

[27] B. Chokkalingam, S. Padmanaban, P. Siano, Z. Leonowicz, and A. Iqbal, A hexagonal hysteresis space vector current controller for single Z-source network multilevel inverter with capacitor balancing, 2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Jun. 2017.

[28] C. Roncero-Clemente, E. Romero-Cadaval, M. Ruiz-Cortes, and O. Husev, Carrier Level-Shifted Based Control Method for the PWM 3L-T-Type qZS Inverter With Capacitor Imbalance Compensation, IEEE Trans. Ind. Electron.,, vol. 65, no. 10, pp. 8297–8306, Oct. 2018.